Stratix IV GX FPGA Development Board

Reference Manual

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Contents

Appendix A. Board Revision History

Additional Information

1. Overview

This document describes the hardware features of the Stratix® IV GX FPGA development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Stratix IV GX FPGA development board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of the Stratix IV GX FPGA designs.

Two High-Speed Mezzanine Card (HSMC) connectors are available to add additional functionality via a variety of HSMC cards available from both Altera and various partners.

To see a list of the latest HSMC cards available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website.

Design advancements and innovations, such as the 8.5 Gbps transceiver modules, the PCI Express hard IP implementation, and programmable power technology ensure that designs implemented in the Stratix IV GX FPGAs operate faster, with lower power than in previous FPGA families.

For more information on the following topics, refer to the respective documents:

- Stratix IV device family, refer to the *Stratix IV Device Handbook*.
- PCI Express MegaCore function, refer to the *PCI Express Compiler User Guide*.
- Altera Video and Image Processing Suite MegaCore functions, refer to the *Video and Image Processing Suite User Guide*.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The board features the following major component blocks:

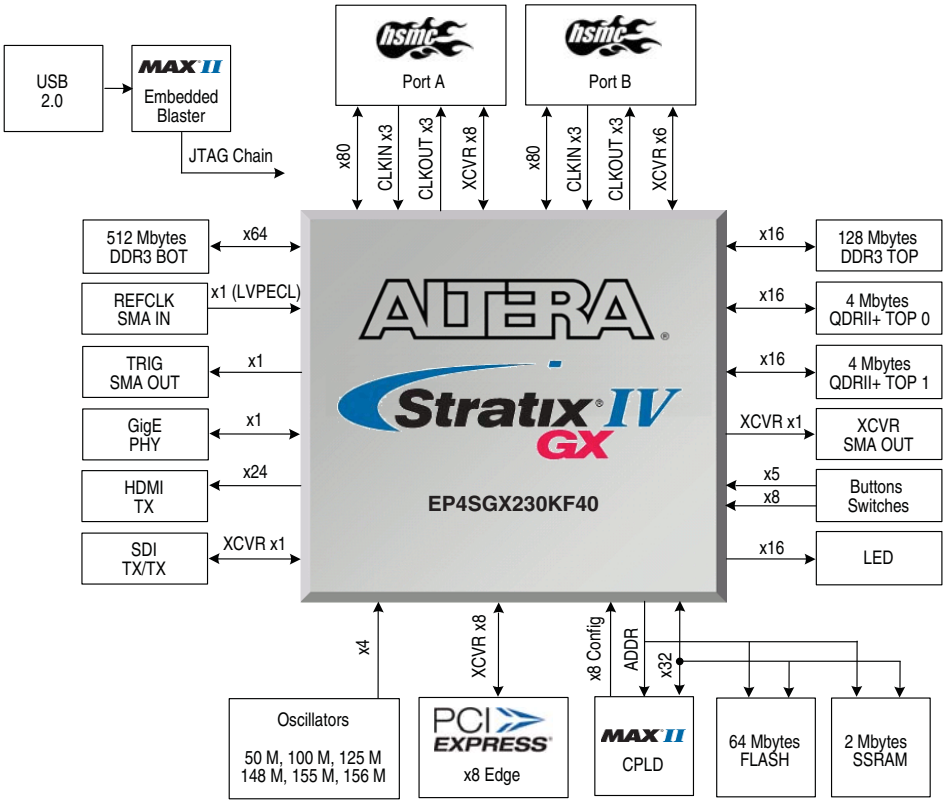
- EP4SGX230KF40 FPGA in the 1517-pin FineLine BGA package
  - 228,000 LEs
  - 91,200 adaptive logic modules (ALMs)
  - 17,133 Kbit (Kb) on-die memory
  - 126.5 Gbps transceivers (PMA only)
  - 2 PCI Express hard IP blocks
  - 8 phase locked loops (PLLs)
  - 1288 18x18 multipliers
  - 0.9-V core power
- MAX® II CPLD EPM2210 System Controller in the 256-pin FineLine BGA Package
  - 1.8-V core power
- FPGA configuration circuitry
  - MAX® II CPLD EPM2210 System Controller and Flash Fast Passive Parallel (FPP) configuration
  - On-Board USB-Blaster™ for use with the Quartus® II Programmer
- On-board clocking circuitry
  - 50-MHz/100-MHz/125-MHz/148.5-MHz/155.52-MHz/156.25-MHz oscillator
  - SMA connectors for external clock input
  - SMA connectors for clock output
- Components and interfaces
  - PCI Express edge connector
  - Gigabit Ethernet
  - HSMC
  - HDMI video port
  - Serial digital interface (SDI) video port
- Memory devices
  - 512-Mbyte (MB) DDR3 SDRAM with a 64-bit data bus (bottom port)
  - 128-MB DDR3 SDRAM with a 16-bit data bus (top port)
  - Two 4-MB QDRII+ SRAMs with 18-bit data buses
  - 2-MB SSRAM with 36-bit data buses
  - 64-MB synchronous flash

- General user I/O
  - 16 user LEDs
  - Two-line character LCD display
  - One configuration done LED
  - One transmit/receive LED (TX/RX) per HSMC interface
  - Four PCI Express LEDs
  - Four Ethernet LEDs
- Push buttons
  - One user reset (CPU reset)
  - One configuration reset
  - Three general user push buttons
- DIP switches
  - Eight user DIP switches
  - Eight MAX II control DIP switches
- Power
  - 16-V – 20-V DC input
  - PCI Express edge connector power
  - On-Board power measurement circuitry
- Mechanical
  - PCI Express half-length full-height (6.6″ x 4.376″)
  - PCI Express chassis or bench-top operation

Development Board Block Diagram

Figure 1–1 shows the block diagram of the Stratix IV GX FPGA development board.

Figure 1–1. Stratix IV GX FPGA Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

Introduction

This chapter introduces all the important components on the Stratix IV GX FPGA development board. Figure 2–1 illustrates major component locations and Table 2–1 provides a brief description of all features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Stratix IV GX development kit documents directory.

For information about powering up the board and installing the demo software, refer to the *Stratix IV GX FPGA Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Stratix IV GX FPGA development board, including an annotated board image and component descriptions. Figure 2–1 provides an overview of the development board features.

Figure 2–1. Overview of the Stratix IV GX FPGA Development Board Features

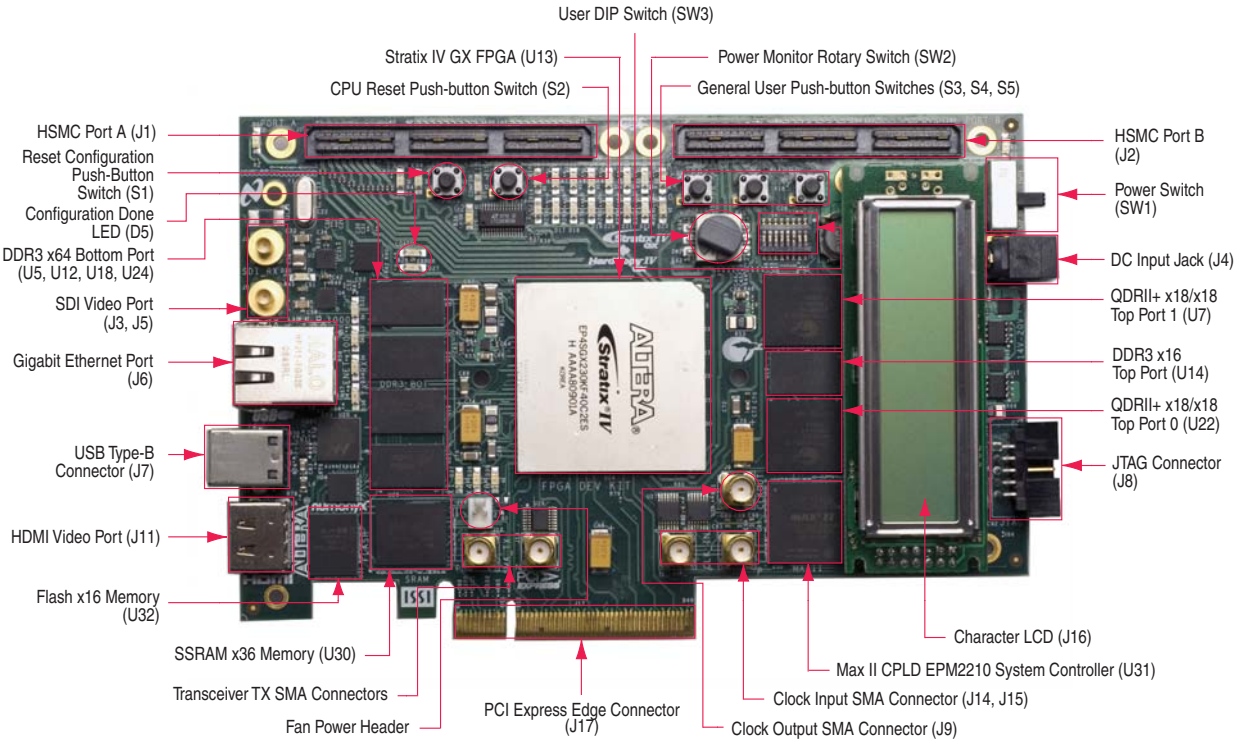


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Stratix IV GX FPGA Development Board Components (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U13	FPGA	EP4SGX230KF40, 1517-pin BGA.
U31	CPLD	EPM2210GF256, 256-pin BGA.
Configuration, Status, and Setup Elements		
SW6	JTAG DIP switch	Enables and disables devices in the JTAG chain.
SW4	Board Settings DIP switch	Controls the Max II CPLD EPM2210 System Controller functions such as clock enable, power and temperature monitor, as well as voltage settings for transceivers and SMA clock input control.
J8	JTAG connector	Disables embedded blaster (for use with external USB-Blasters).
SW5	PCI Express DIP switch	Controls the PCI Express lane width by connecting `prsnt` pins together on the PCI Express edge connector.
D5	Configuration done LED	Illuminates when the FPGA is configured.

Table 2–1. Stratix IV GX FPGA Development Board Components (Part 2 of 3)

Board Reference	Type	Description
D26	Load LED	Illuminates during embedded USB-Blaster data transfers.
D27	Error LED	Illuminates when the FPGA configuration from flash fails.
D24	Power LED	Illuminates when 12-V power is present.
D32, D33, D34, D35	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D3, D4	HSMC port A LEDs	You can configure these LEDs to indicate transmit or receive activity.
D1	HSMC port A Present LED	Illuminates when a daughtercard is plugged into the HSMC port A.
D14, D15	HSMC port B LEDs	You can configure these LEDs to indicate transmit or receive activity.
D2	HSMC port B Present LED	Illuminates when a daughtercard is plugged into the HSMC port B.
D30	SDI mute LED	Illuminates when the SDI receiver is muted.
D25	PCI Express Gen 2 LED	You can configure this LED to illuminate when PCI Express is in Gen 2 mode.
D37, D38, D39	PCI Express Link LEDs	You can configure these LEDs to display the PCI Express link width (x1, x4, x8).
Clock Circuitry		
X1	125 M oscillator	125.000-MHz crystal oscillator for Gigabit Ethernet, Serial RapidIO™ (SRIO), or PCI Express.
X2	156 M oscillator	156.250-MHz crystal oscillator for 10 Gigabit Ethernet or XAUI.
X3	148 M oscillator	148.500-MHz voltage controlled crystal oscillator for SDI Video.
X6	100 M oscillator	100.000-MHz crystal oscillator for PCI Express or general use such as memories. Multiplex with CLKIN_SMA_P based on CLK_SEL switch value.
X7	155 M oscillator	155.520-MHz crystal oscillator for SONET.
X8	50 M oscillator	50.000-MHz crystal oscillator for general purpose logic.
J15, J14	Clock input SMAs	Drives LVPECL-compatible clock inputs into the U50 clock multiplexer buffer.
J9	Clock output SMA	Drives out 2.5-V CMOS clock outputs from the FPGA.
General User Input and Output		
D6-D13 D16-D23	User LEDs	16 user LEDs. Illuminates when driven low.
SW3	User DIP switch	Octal user DIP switches. When the switch is ON, a logic 0 is selected.
S1	Reset configuration push button	Reconfigures the FPGA from the flash memory.
S2	CPU reset push button	Resets the Max II CPLD EPM2210 System Controller and FPGA logic.
S3, S4, S5	General user push buttons	Three user push buttons. Driven low when pressed.
SW2	Power monitor rotary switch	Selects the power rail being measured and also the FPGA image to load on power-up; 0 selects factory image and 1 selects user-defined image.
Memory Devices		
U5, U12, U18, U24	DDR3 x64 bottom port	A single 64-bit 512-MB memory port.
U14	DDR3 x16 top port	Independent 16-bit 128-MB memory port.

Table 2–1. Stratix IV GX FPGA Development Board Components (Part 3 of 3)

Board Reference	Type	Description
U22	QDRII+ x18/x18 top port 0	18-bit read and 18-bit write 4-MB SRAM port.
U7	QDRII+ x18/x18 top port 1	Second 18-bit read and 18-bit write 4-MB SRAM port.
U30	SSRAM x36 memory	Standard synchronous RAM which makes a 36-bit 2-MB SRAM port.
U32	Flash x16 memory	Synchronous burst mode flash device which provides a 16-bit 64-MB non-volatile memory port.
Communication Ports		
J17	PCI Express edge connector	Connector with gold-plated edge fingers for up to ×8 signaling in either Gen1 or Gen2 mode.
J1	HSMC port A	Provides eight transceiver channels and 84 CMOS or 17 LVDS channels per the HSMC specification.
J2	HSMC port B	Provides six transceiver channels and 84 CMOS or 17 LVDS channels per the HSMC specification.
J7	USB Type-B connector	Embedded USB-Blaster JTAG for programming the FPGA via a type-B USB cable.
J6	Gigabit Ethernet port	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in SGMII mode.
Video and Display Ports		
J11	HDMI video port	19-pin HDMI connector which provides a HDMI video output of up to 1080i through an AD9889B PHY.
J3, J5	SDI video port	Two 75-Ω system management bus (SMB) connectors which provide a full-duplex SDI interface through a LMH0302 driver and LMH0344 cable equalizer.
J16	Character LCD	Connector which interfaces to the provided 16 character × 2 line LCD module along with standoffs S1 and S2.
Power Supply		
J17	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J4	DC input jack	Accepts a 14-V – 20-V DC power supply.
SW1	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Stratix IV GX Device

The Stratix IV GX FPGA development board features the Stratix IV GX EP4SGX230KF40 device (U13) in a 1517-pin FineLine BGA package.

For more information about the Stratix IV device family, refer to the *Stratix IV Device Handbook*.

Table 2–2 describes the features of the Stratix IV GX EP4SGX230KF40 device.

Table 2–2. Stratix IV GX Device EP4SGX230KF40 Features

ALMs	Equivalent LEs	M9K RAM Blocks	M144K Blocks	MLAB Blocks	Total RAM Kbits	18-bit × 18-bit Multipliers	PLLs	Transceivers (8.5 Gbps, 3.2 Gbps)	Package Type
91,200	228,000	1,235	22	4,560	17,133	1288	8	24, 12	1517-pin FineLine BGA

Table 2–3 lists the Stratix IV GX component reference and manufacturing information.

Table 2–3. Stratix IV GX Device Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U13	FPGA, Stratix IV GX F1517, 228K LES, leadfree	Altera Corporation	EP4SGX230KF40C2N	www.altera.com

I/O Resources

Figure 2–2 shows the bank organization and I/O count for the EP4SGX230 device in the 1517-pin FineLine BGA package.

Figure 2–2. EP4SGX230KF40 Device I/O Bank Diagram

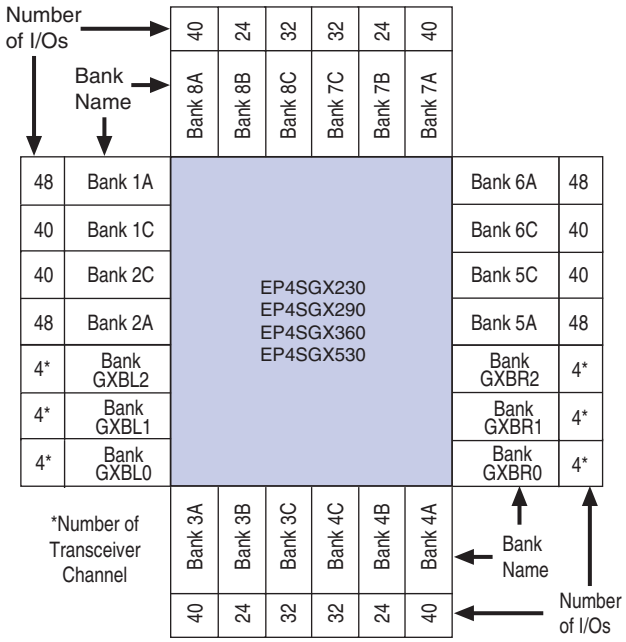


Table 2–4 lists the Stratix IV GX device pin count and usage by function on the development board.

Table 2–4. Stratix IV GX Device Pin Count and Usage (Part 1 of 2)

Function	I/O Standard	I/O Count	Special Pins
DDR3 ×16 Top Port	1.5-V SSTL	49	2 Diff ×8 DQS
DDR3 ×64 Bottom Port	1.5-V SSTL	117	8 Diff ×8 DQS
QDRII+ Top Port 0	1.5-V HSTL	66	1 Diff ×18 DQS
QDRII+ Top Port 1	1.5-V HSTL	66	1 Diff ×18 DQS
Flash, SRAM, MAX FSM Bus	2.5-V CMOS	78	—
PCI Express ×8	2.5-V CMOS + XCVR	38	1 REFCLK, 8 XCVR
HSMC Port A	2.5-V CMOS + LVDS + XCVR	116	8 XCVR, 17 LVDS, 5 Clock Inputs
HSMC Port B	2.5-V CMOS + LVDS + XCVR	116	6 XCVR, 17 LVDS, 5 Clock Inputs
Gigabit Ethernet	2.5-V CMOS + LVDS	8	1 LVDS
HDMI Video	2.5-V CMOS	39	—
SDI Video	XCVR	7	1 XCVR
Buttons	2.5-V CMOS	4	1 DEV_CLRn
Switches	2.5-V CMOS	8	—
LCD	2.5-V CMOS	11	—
LEDs	2.5-V CMOS	24	—

Table 2–4. Stratix IV GX Device Pin Count and Usage (Part 2 of 2)

Function	I/O Standard	I/O Count	Special Pins
Clocks or Oscillators	2.5-V CMOS + LVDS	11	4 REFCLK
Power or Temperature Sense	2.5-V CMOS10	10	1 tempdiode_p, 1 tempdiode_n
Device I/O Total:		768	

Migration Support

Although the target FPGA for this development board is the EP4SGX230KF40 device, the first device released in this 40nm FPGA family, the board supports migration to the largest Stratix IV GX device, the EP4SGX530KF40.

Table 2–5 describes the features of the Stratix IV GX EP4SGX530KF40 device.

Table 2–5. Stratix IV GX Device EP4SGX530KF40 Features

ALMs	Equivalent LEs	M9K RAM Blocks	M144K Blocks	MLAB Blocks	Total RAM Kbits	18-bit × 18-bit Multipliers	PLLs	Transceivers (8.5 Gbps, 3.2 Gbps)	Package Type
212,480	531,200	1,280	64	10,624	27,376	1024	8	24, 12	1517-pin Fineline BGA

The specific I/O resources available in the Stratix IV GX EP4SGX230KF40 device are the same for the Stratix IV GX EP4SGX530KF40 device.

MAX II CPLD EPM2210 System Controller

The board utilizes the EPM2210 System Controller, an Altera MAX II CPLD, for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Temperature monitoring
- Fan control
- Virtual JTAG interface for PC-based power and temperature GUI
- Control registers for clocks
- Control registers for remote system update
- Control registers for SDI, SRAM, and fan speed.
- Register with CPLD design revision and board information (read-only)

Figure 2–3 illustrates the MAX II CPLD EPM2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–3. MAX II CPLD EPM2210 System Controller Block Diagram

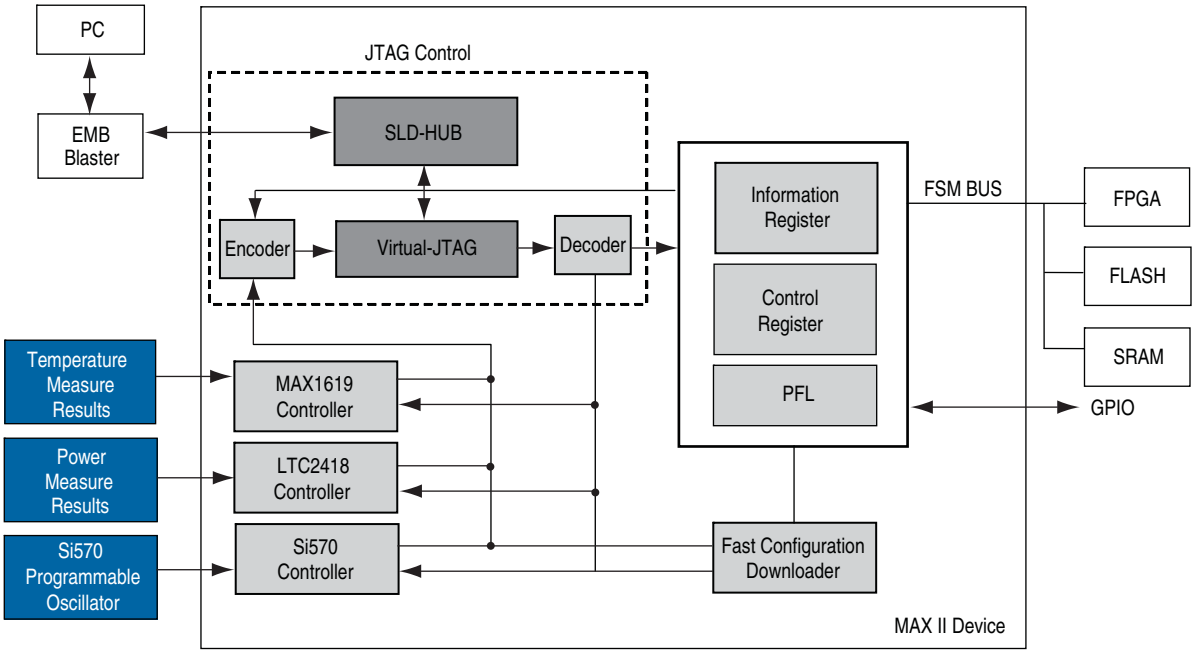


Table 2–6 lists the I/O signals present on the MAX II CPLD EPM2210 System Controller. The signal names and functions are relative to the MAX II device (U30).

Table 2–6. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 1 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4SGX230 Pin Number	Description
FSM_A25	2.5-V	D5	AP30	FSM bus address
FSM_A24	2.5-V	B1	AN30	FSM bus address
FSM_A23	2.5-V	D4	AL31	FSM bus address
FSM_A22	2.5-V	B9	AK31	FSM bus address
FSM_A21	2.5-V	D9	AR32	FSM bus address
FSM_A20	2.5-V	A10	AP32	FSM bus address
FSM_A19	2.5-V	C9	AH29	FSM bus address
FSM_A18	2.5-V	B10	AG29	FSM bus address
FSM_A17	2.5-V	A11	AR35	FSM bus address
FSM_A16	2.5-V	E10	AP35	FSM bus address
FSM_A15	2.5-V	B11	AL32	FSM bus address
FSM_A14	2.5-V	D10	AK32	FSM bus address
FSM_A13	2.5-V	A12	AU33	FSM bus address
FSM_A12	2.5-V	C10	AT33	FSM bus address
FSM_A11	2.5-V	B12	AH30	FSM bus address

Table 2–6. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 2 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4SGX230 Pin Number	Description
FSM_A10	2.5-V	E11	AJ31	FSM bus address
FSM_A9	2.5-V	A13	AR34	FSM bus address
FSM_A8	2.5-V	D11	AT34	FSM bus address
FSM_A7	2.5-V	B13	AE27	FSM bus address
FSM_A6	2.5-V	C11	AD27	FSM bus address
FSM_A5	2.5-V	B14	AP34	FSM bus address
FSM_A4	2.5-V	D12	AN33	FSM bus address
FSM_A3	2.5-V	A15	AD26	FSM bus address
FSM_A2	2.5-V	C12	AC26	FSM bus address
FSM_A1	2.5-V	B16	AP33	FSM bus address
FSM_A0	2.5-V	C13	AN32	FSM bus address
FSM_D31	2.5-V	T13	T28	FSM bus data
FSM_D30	2.5-V	N11	R28	FSM bus data
FSM_D29	2.5-V	R12	F32	FSM bus data
FSM_D28	2.5-V	M11	E32	FSM bus data
FSM_D27	2.5-V	T12	L31	FSM bus data
FSM_D26	2.5-V	P10	K31	FSM bus data
FSM_D25	2.5-V	R11	F31	FSM bus data
FSM_D24	2.5-V	N10	E31	FSM bus data
FSM_D23	2.5-V	T11	N29	FSM bus data
FSM_D22	2.5-V	M10	M29	FSM bus data
FSM_D21	2.5-V	T10	H31	FSM bus data
FSM_D20	2.5-V	P9	G31	FSM bus data
FSM_D19	2.5-V	R9	N30	FSM bus data
FSM_D18	2.5-V	T9	M30	FSM bus data
FSM_D17	2.5-V	T8	D33	FSM bus data
FSM_D16	2.5-V	N9	C33	FSM bus data
FSM_D15	2.5-V	C7	N31	FSM bus data
FSM_D14	2.5-V	B5	M31	FSM bus data
FSM_D13	2.5-V	D7	C32	FSM bus data
FSM_D12	2.5-V	A5	B32	FSM bus data
FSM_D11	2.5-V	E7	J32	FSM bus data
FSM_D10	2.5-V	B6	H32	FSM bus data
FSM_D9	2.5-V	A6	D35	FSM bus data
FSM_D8	2.5-V	C8	C35	FSM bus data
FSM_D7	2.5-V	B7	N28	FSM bus data
FSM_D6	2.5-V	D8	M28	FSM bus data
FSM_D5	2.5-V	A7	D31	FSM bus data
FSM_D4	2.5-V	E8	C31	FSM bus data

Table 2–6. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 3 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4SGX230 Pin Number	Description
FSM_D3	2.5-V	B8	K30	FSM bus data
FSM_D2	2.5-V	A8	J30	FSM bus data
FSM_D1	2.5-V	A9	D34	FSM bus data
FSM_D0	2.5-V	E9	C34	FSM bus data
MAX2_CLK	2.5-V	E1	K32	FSM bus MAX2 clock
MAX2_WEn	2.5-V	F4	T27	FSM bus MAX2 write enable
MAX2_CSn	2.5-V	E2	E34	FSM bus MAX2 chip select
MAX2_OEn	2.5-V	F3	J33	FSM bus MAX2 output enable
MAX2_BEn3	2.5-V	F1	R27	FSM bus MAX2 byte enable 3
MAX2_BEn2	2.5-V	F6	P29	FSM bus MAX2 byte enable 2
MAX2_BEn1	2.5-V	F2	F34	FSM bus MAX2 byte enable 1
MAX2_BEn0	2.5-V	F5	H34	FSM bus MAX2 byte enable 0
FLASH_CLK	2.5-V	C6	AF26	FSM bus flash clock
FLASH_WEn	2.5-V	A4	AT31	FSM bus flash write enable
FLASH_CEn	2.5-V	E6	AU31	FSM bus flash chip enable
FLASH_OEn	2.5-V	B4	AG27	FSM bus flash output enable
FLASH_RDYBSYn	2.5-V	D6	AT32	FSM bus flash ready
FLASH_RESETn	2.5-V	C4	AL30	FSM bus flash reset
FLASH_ADVn	2.5-V	B3	AN31	FSM bus flash address valid
FPGA_CONFIG_D7	2.5-V	D1	R34	FPGA configuration data
FPGA_CONFIG_D6	2.5-V	E5	R35	FPGA configuration data
FPGA_CONFIG_D5	2.5-V	D2	W26	FPGA configuration data
FPGA_CONFIG_D4	2.5-V	E4	V27	FPGA configuration data
FPGA_CONFIG_D3	2.5-V	C3	P34	FPGA configuration data
FPGA_CONFIG_D2	2.5-V	E3	N35	FPGA configuration data
FPGA_CONFIG_D1	2.5-V	C2	W29	FPGA configuration data
FPGA_CONFIG_D0	2.5-V	D3	W30	FPGA configuration data
FPGA_DCLK	2.5-V	H4	AR11	FPGA configuration clock
FPGA_nSTATUS	2.5-V	H3	AW35	FPGA configuration ready
FPGA_nCONFIG	2.5-V	T2	AW36	FPGA configuration active
FPGA_CONF_DONE	2.5-V	J1	AV35	FPGA configuration done
SENSE_SCK	2.5-V	L5	AE28	Power monitor SPI clock
SENSE_SDI	2.5-V	M3	J35	Power monitor SPI data in
SENSE_SDO	2.5-V	L4	V28	Power monitor SPI data out
SENSE_CS0n	2.5-V	N1	AB31	Power monitor 0 chip select
SENSE_CS1n	2.5-V	L3	H35	Power monitor 1 chip select
SENSE_ADN_F0	2.5-V	N2	G35	Power monitor frequency
SENSE_SMB_CLK	2.5-V	R1	W34	Temperature monitor SMB clock
SENSE_SMB_DATA	2.5-V	R4	AH32	Temperature monitor SMB data

Table 2–6. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 4 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4SGX230 Pin Number	Description
OVERTEMPn	2.5-V	P5	—	Temperature monitor over-temperature indicator
ALERTn	2.5-V	M2	—	Temperature monitor alert
PHASE_0	2.5-V	T6	—	Power clock 0 degrees
PHASE_90	2.5-V	R7	—	Power clock 90 degrees
PHASE_135	2.5-V	P8	—	Power clock 135 degrees
PHASE_270	2.5-V	T7	—	Power clock 270 degrees
MAX_ERROR	2.5-V	G3	—	FPGA configuration error LED
MAX_LOAD	2.5-V	G2	—	FPGA configuration active LED
MAX_CONF_DONEn	2.5-V	E15	—	FPGA configuration done LED
USB_LED	2.5-V	F12	—	Embedded USB-Blaster active
HSMA_PRSNTn	2.5-V	J16	—	HSMC port A present
HSMB_PRSNTn	2.5-V	J13	—	HSMC port B present
MAX_DIP	2.5-V	F15	—	DIP-reserved
USB_DISABLEn	2.5-V	G14	—	DIP-embedded USB-Blaster disable
LCD_PWRMON	2.5-V	R5	—	DIP-MAX2 LCD drive enable
FAN_FORCE_ON	2.5-V	P7	—	DIP-force fan on switch
CLK_SEL	2.5-V	T5	—	DIP-clock select SMA or oscillator
CLK_ENABLE	2.5-V	N7	—	DIP-clock oscillator enable
PGM3	2.5-V	J3	—	Rotary switch input
PGM2	2.5-V	K1	—	Rotary switch input
PGM1	2.5-V	J4	—	Rotary switch input
PGM0	2.5-V	J2	—	Rotary switch input
RESET_CONFIGn	2.5-V	K2	—	Force FPGA configuration push-button switch
CPU_RESETn	2.5-V	M9	V34	Reset push button
SRAM_MODE	2.5-V	P4	—	SRAM mode
SRAM_ZZ	2.5-V	L14	—	SRAM sleep mode
CLK50_EN	2.5-V	G12	—	50 MHz oscillator enable
CLK100_EN	2.5-V	G16	—	100 MHz oscillator enable
CLK100_SDA	2.5-V	A2	—	100 MHz programming data
CLK100_SCL	2.5-V	C15	—	100 MHz programming clock
CLK125_EN	2.5-V	H16	—	125 MHz oscillator enable
CLK148_EN	2.5-V	H13	—	148 MHz oscillator enable
CLK155_EN	2.5-V	H15	—	155 MHz oscillator enable
CLK156_EN	2.5-V	H14	—	156 MHz oscillator enable
CLKIN_50	2.5-V	J5	AC34	50 MHz clock input
CLK_CONFIG	2.5-V	J12	—	125 MHz configuration clock

Table 2–7 lists the MAX II CPLD EPM2210 System Controller component reference and manufacturing information.

Table 2–7. MAX II CPLD EPM2210 System Controller Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U30	IC - MAX II CPLD EPM2210 256FBGA -3 LF 1.8V VCCINT	Altera Corporation	EPM2210GF256C3N	www.altera.com

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

This section describes the FPGA, flash memory, and MAX II CPLD EPM2210 System Controller device programming methods supported by the Stratix IV GX FPGA development board. The Stratix IV GX FPGA development board supports three configuration methods:

- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- Flash memory download for configuring the FPGA using stored images from the flash memory on either power-up or by pressing the reset configuration push button (S1).
- External USB-Blaster for configuring the FPGA using an external USB-Blaster.

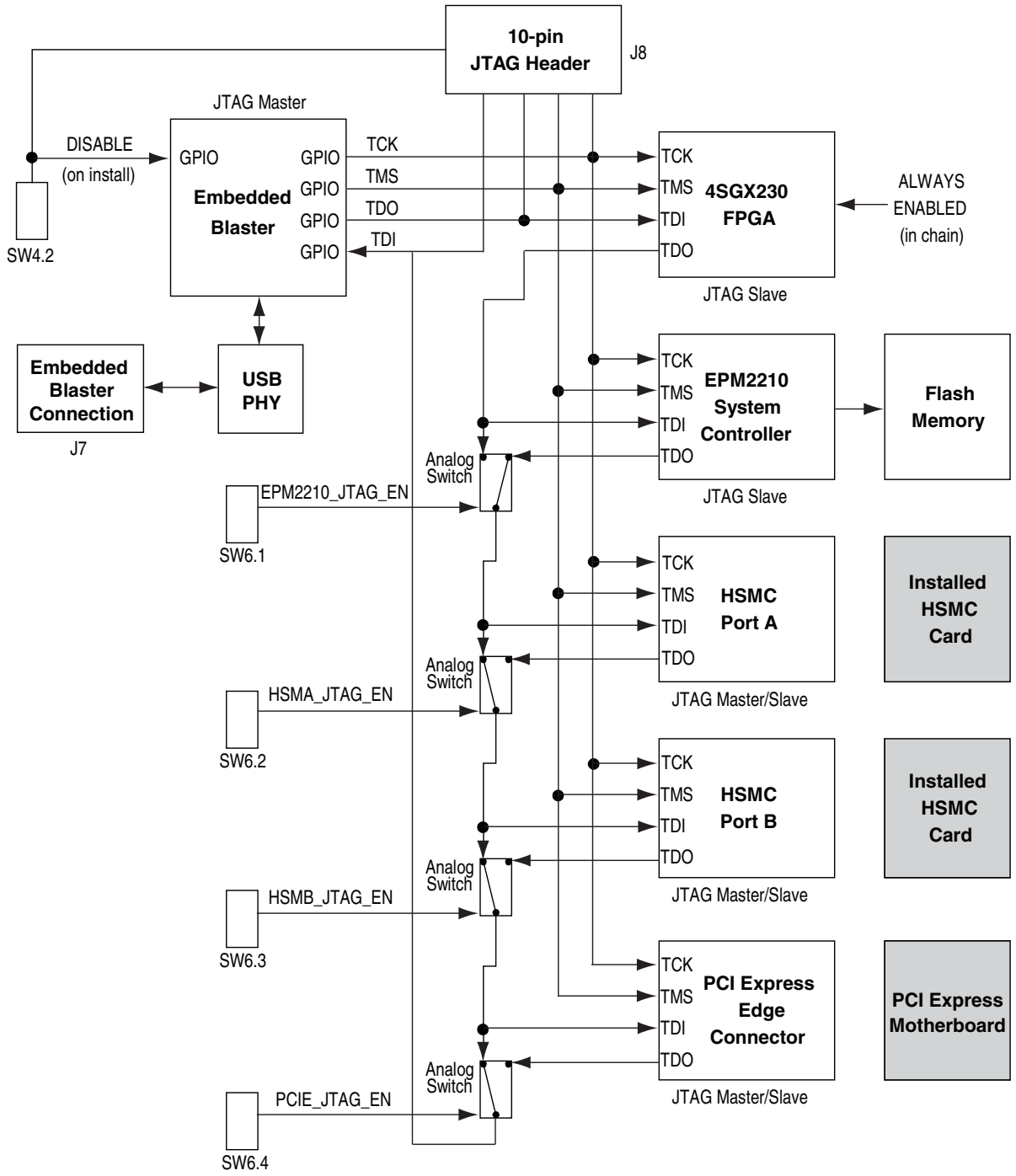
FPGA Programming over Embedded USB-Blaster

The USB-Blaster is implemented using a type-B USB connector (J7), a FTDI USB 2.0 PHY device (U39), and an Altera MAX II CPLD (U30). This method allows the configuration of the FPGA using a USB cable that connects directly between the USB port on the board (J7) and a USB port of a PC running the Quartus II software. The embedded USB-Blaster found in the MAX II CPLD EPM2210 System Controller normally masters the JTAG chain.

The embedded USB-Blaster is automatically disabled when an external USB-Blaster connects to the JTAG chain.

Figure 2–4 illustrates the JTAG chain.

Figure 2–4. JTAG Chain



Each jumper shown in Figure 2–4 is located in the JTAG DIP switch (SW6) on the back of the board. To connect a device or interface in the chain, their corresponding switch must be in the down position. Push all the switches in the up position to only have the FPGA in the chain.

The MAX II CPLD EPM2210 System Controller must be in the chain to use some of the GUI interfaces. For this setting, push the left-most switch in the down position and all other switches in the up position.

Flash Programming

Flash programming is possible through a variety of methods using the Stratix IV GX device.

The default method is to use the factory design called the Board Update Portal. This design is an embedded webserver, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash over the network.

The secondary method is to use the pre-built PFL design included in the development kit. The development board implements the Altera PFL megafunction for flash programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash can be used as well, including the Nios® II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

FPGA Programming from Flash Memory

On either power-up or by pressing the reset configuration push button (S1), the MAX II CPLD EPM2210 System Controller's parallel flash loader (PFL) configures the FPGA from the flash memory. The PFL megafunction reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 8-bit data is then written to the FPGA's dedicated configuration pins during configuration.

Figure 2–5 shows the PFL configuration.

Figure 2–5. PFL Configuration

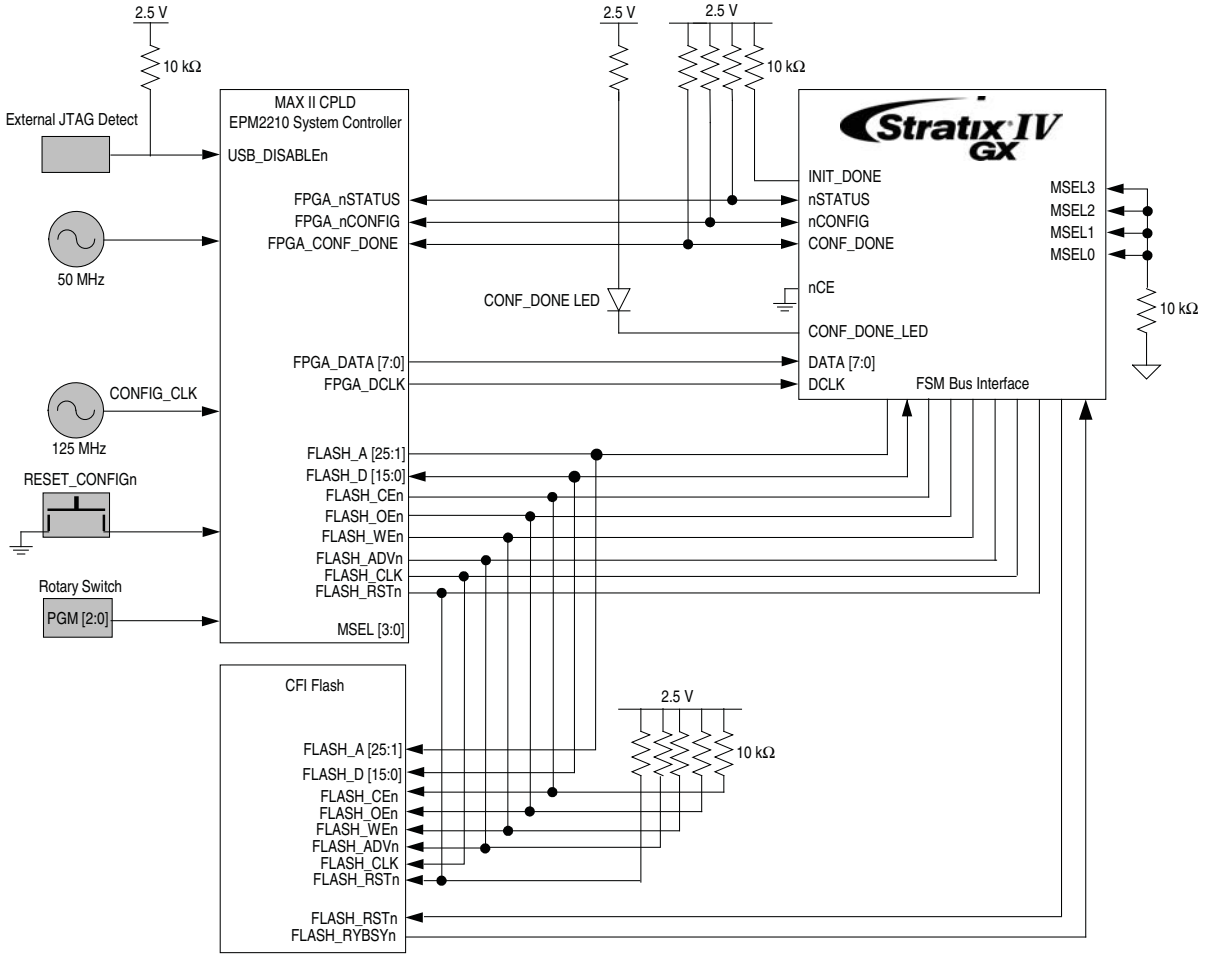


Table 2–8 lists the flash memory map storage.

Table 2–8. Flash Memory Map (Part 1 of 2)

Name	Size (Kbyte)	Address
Unused	32	0x03FF.FFFF 0x03FF.8000
	32	0x03FF.7FFF 0x03FF.0000
	32	0x03FE.FFFF 0x03FE.8000
	32	0x03FE.7FFF 0x03FE.0000
User Software	24,320	0x03FD.FFFF 0x0282.0000

Table 2–8. Flash Memory Map (Part 2 of 2)

Name	Size (Kbyte)	Address
Factory Software	8,192	0x0281.FFFF 0x0202.0000
zipfs — HTML, Web Content	8,192	0x0201.FFFF 0x0182.0000
User Hardware	12,288	0x0181.FFFF 0x00C2.0000
Factory Hardware	12,288	0x00C1.FFFF 0x0002.0000
PFL Option Bits	32	0x0001.FFFF 0x0001.8000
Board Information	32	0x0001.7FFF 0x0001.0000
Ethernet Option Bits	32	0x0000.FFFF 0x0000.8000
User Design Reset Vector	32	0x0000.7FFF 0x0000.0000

There are two pages reserved for the FPGA configuration data. The factory hardware page (page 0) loads if the rotary switch is in position 0 and when either power is cycled or the reset configuration push button (S1) is pressed. The user hardware page (page 1) loads if the rotary switch is in position 1 and when either power is cycled or the reset configuration push button (S1) is pressed.

FPGA Programming over External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA (U13) using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG connector (J8). The JTAG DIP switch (SW6) allows the MAX II CPLD device to be removed from the JTAG chain so that the FPGA is the only device on the JTAG chain.

For more information on the following topics, refer to the respective documents:

- Board Update Portal, refer to the *Stratix IV GX FPGA Development Kit User Guide*.
- PFL design, refer to the *Stratix IV GX FPGA Development Kit User Guide*.
- PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software.*

Status Elements

The development board includes status LEDs. This section describes the status elements.

Table 2–9 lists the LED board references, names, and functional descriptions.

Table 2–9. Board-Specific LEDs

Board Reference	LED Name	Description
D24	POWER	Blue LED. Illuminates when 3.3-V power is active.
D5	CONF DONE	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D26	Loading	Green LED. Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD EPM2210 System Controller wire-OR'd with the Embedded Blaster CPLD.
D27	Error	Red LED. Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D35	ENET TX	Green LED. Blinks to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D34	ENET RX	Green LED. Blinks to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.
D33	100	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed Driven by the Marvell 88E1111 PHY.
D32	1000	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D1	HSMC Port A Present	Green LED. Illuminates when the HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D2	HSMC Port B Present	Green LED. Illuminates when the HSMC port B has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D30	MUTE	Green LED. Illuminates when the SDI receiver carrier detect is active.
D40	FAN LED	Green LED. Illuminates when a heat sink or fan should be installed. Driven by the MAX1619 thermal sensor `OVERTEMPn` signal.

Table 2–10 lists the board-specific LEDs component references and manufacturing information.

Table 2–10. Board-Specific LEDs Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D1, D2, D26	Green LEDs	Lumex Inc.	SML-LX1206GC-TR	www.lumex.com
D27	Red LED	Lumex Inc.	SML-LX1206USBC-TR	www.lumex.com
D24	Blue LED	Lumex Inc.	SML-LX1206USBC-TR	www.lumex.com

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG control DIP switch
- PCI Express control DIP switch
- Reset configuration push button
- Rotary switch

Board Settings DIP Switch

The board settings DIP switch controls various features specific to the board and the MAX II CPLD EPM2210 System Controller logic design. Table 2–11 lists the switch controls and descriptions.

Table 2–11. Board Settings DIP Switch Controls

Switch	Schematic Signal Name	Description	Default
1	MAX_DIP	Reserved	OFF
2	USB_DISABLEn	ON : Embedded USB-Blaster disabled OFF : Embedded USB-Blaster enabled	OFF
3	LCD_PWRMON	ON : LCD driven from the Max II EPM2210 System Controller (power monitor) OFF : LCD driven from the FPGA (no power monitor)	ON
4	FAN_FORCE_ON	ON : Fan forced ON OFF : Fan speed controlled by the MAX1619 device	OFF
5	CLK_SEL	ON : 100 MHz oscillator input select OFF : SMA input select	ON
6	CLK_ENABLE	ON : On-Board oscillator enabled OFF : On-Board oscillator disabled	ON
7	S4VCCH_SEL	ON : 1.4 V (default) OFF : Reserved	ON
8	S4VCCA_SEL	ON : 3.3 V (default) OFF : 2.5 V	ON

Table 2–12 lists the board settings DIP switch component reference and manufacturing information.

Table 2–12. Board Settings DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW4	Eight-position slide DIP switch	C & K Components	TDA08H0SB1	www.ck-components.com

JTAG Control DIP Switch

The JTAG control DIP switch can either remove or include devices in the active JTAG chain. However, the Stratix IV GX FPGA device is always in the JTAG chain. Table 2–13 lists the switch controls and its descriptions.

Table 2–13. JTAG Control DIP Switch Controls

Switch	Schematic Signal Name	Description	Default
1	EPM2210_JTAG_EN	ON : Bypass Max II CPLD EPM2210 System Controller OFF : Max II CPLD EPM2210 System Controller in-chain	ON
2	HSMA_JTAG_EN	ON : Bypass HSMA OFF : HSMA in-chain	ON
3	HSMB_JTAG_EN	ON : Bypass HSMB OFF : HSMB in-chain	ON
4	PCIE_JTAG_EN	ON : Bypass PCI Express OFF : Reserved (disables JTAG chain, do not use)	ON

Table 2–14 lists the JTAG control DIP switch component references and manufacturing information.

Table 2–14. JTAG Control DIP Switch Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW6	Four-position slide DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com

PCI Express Control DIP Switch

The PCI Express control DIP switch can enable or disable the different configurations. Table 2–15 lists the switch controls and descriptions.

Table 2–15. PCI Express Control DIP Switch Controls

Switch	Schematic Signal Name	Description	Default
1	PCIE_PRSNT2n_x1	ON : Enable x1 presence detect OFF : Disable x1 presence detect	ON
2	PCIE_PRSNT2n_x4	ON : Enable x4 presence detect OFF : Disable x4 presence detect	ON
3	PCIE_PRSNT2n_x8	ON : Enable x8 presence detect OFF : Disable x8 presence detect	ON
4	MAX_EN	Reserved	OFF

Table 2–16 lists the PCI Express control DIP switch component reference and manufacturing information.

Table 2–16. PCI Express Control DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW5	Four-Position slide DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com

Reset Configuration Push Button

The reset configuration push button, RESET_CONFIGn, is an input to the MAX II CPLD EPM2210 System Controller. The push button forces a reconfiguration of the FPGA from flash memory. The location in the flash memory is based on the input from the rotary switch position when you release the push button. Valid locations include 0 and 1 for the two pages in flash reserved for FPGA designs.

Table 2–17 lists the reset configuration push button component reference and manufacturing information.

Table 2–17. Reset Configuration Push Button Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S1	Push button	Panasonic Corporation	EVQPAC07K	www.panasonic.com

Rotary Switch

The 16-position rotary switch (SW2) is wired to the MAX II CPLD EPM2210 System Controller. This rotary switch serves the following purposes:

- At power up or when you press the reset configuration push button (S1), this switch selects either the factory (page 0) or the user (page 1) design to load into the FPGA.
- After power up, the rotary switch selects the power rail monitored from among a total of 16 rails. The power information is displayed in the Power GUI on a host PC with a USB connection to the board.
- User applications can obtain the switch value by reading the rsr register over the FSM bus in the MAX II CPLD EPM2210 System Controller.

Table 2–18 lists the power rails that are measured based on the rotary switch position.

Table 2–18. Power Rail Measurements Based on the Rotary Switch Position (Part 1 of 2)

Switch	Schematic Signal Name	Voltage (V)	Device Pin	Description
0	S4VCCIO_B7B8	1.5	VCCIO_B7	Bank 7 I/O power (QDR2TOP0+DDR)
			VCCIO_B8	Bank 8 I/O power (QDR2TOP1+DDR)
1	S4VCC	0.90	VCC	FPGA core and periphery power
			VCCHIP	PCI Express hard IP block
2	3.3 V	3.3	—	All 3.3 V power to board (mA only)

Table 2–18. Power Rail Measurements Based on the Rotary Switch Position (Part 2 of 2)

Switch	Schematic Signal Name	Voltage (V)	Device Pin	Description
3	S4VCCIO_INT	2.5	VCCPD	I/O pre-drivers
			VCCPGM	Configuration I/O
			VCC_CLKIN	V_{cc} clock input pins
4	S4VCCH_GXB	1.4	VCCH_GXB	XCVR clock buffers
5	S4VCCAUX	2.5	VCCAUX	Programmable power tech auxiliary
			VCCA_PLL	PLL analog
6	S4VCCPT	1.5	VCCPT	Programmable power tech
7	S4VCCD_PLL	0.90	VCCD_PLL	PLL digital
8	S4VCCA_GXB	3.0	VCCA_GXB	XCVR analog TX/RX driver (mA only)
9	S4VCCIO_B5	2.5	VCCIO_B5	Bank 5 I/O power (HSMC port A)
A	S4VCCIO_B6	2.5	VCCIO_B6	Bank 6 I/O power (HSMC port B)
B	S4VCCIO_B1B2	2.5	VCCIO_B1	Bank 1 I/O power (FSM bus)
			VCCIO_B2	Bank 2 I/O power (FSM bus)
C	S4VCCIO_B3A	1.8	VCCIO_B3A	Bank 3A I/O power (HDMI)
D	S4VCCIO_B3B4	1.5	VCCIO_B3	Bank 3 I/O power (DDR3BOT)
			VCCIO_B4	Bank 4 I/O power (DDR3BOT)
E	S4VCC_GXB	1.1	VCCR	XCVR analog receive
			VCCT	XCVR analog transmit
			VCCL_GXB	XCVR clock distribution
F	12 V	12	—	All 12 V power

Table 2–19 lists the rotary switch component reference and manufacturing information.

Table 2–19. Rotary Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW2	16-position rotary switch	Grayhill Corporation	94HCB16WT	www.grayhill.com

Clock Circuitry

This section describes the board's clock inputs and outputs.

Stratix IV GX FPGA Clock Inputs

The development board has two types of clock inputs: global clock inputs and transceiver reference clock inputs.

Figure 2–6 shows the Stratix IV GX FPGA development board global clock inputs. The Stratix IV GX FPGA development board transceiver reference clock inputs are shown in Figure 2–7.

Figure 2–6. Stratix IV GX FPGA Development Board Global Clock Inputs

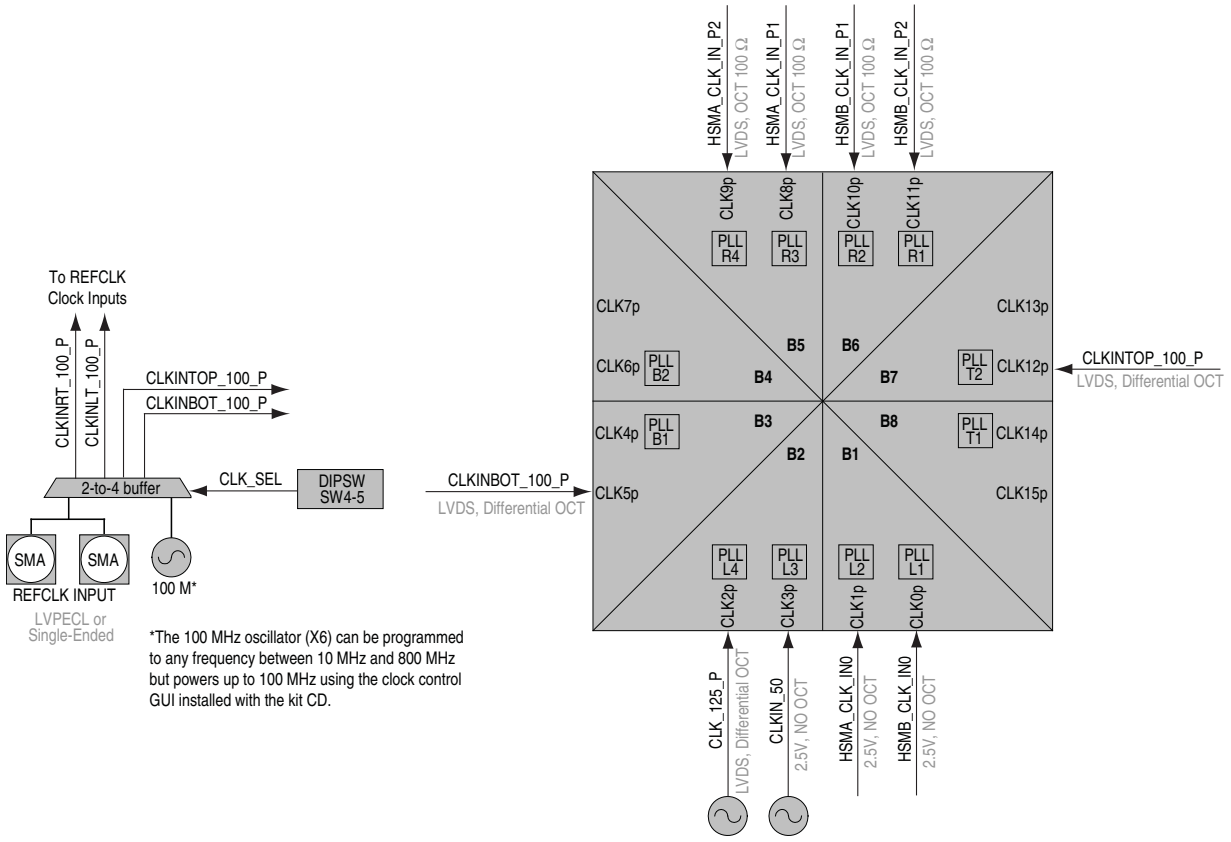


Figure 2–7. Stratix IV GX FPGA Development Board Transceiver Reference Clock Inputs

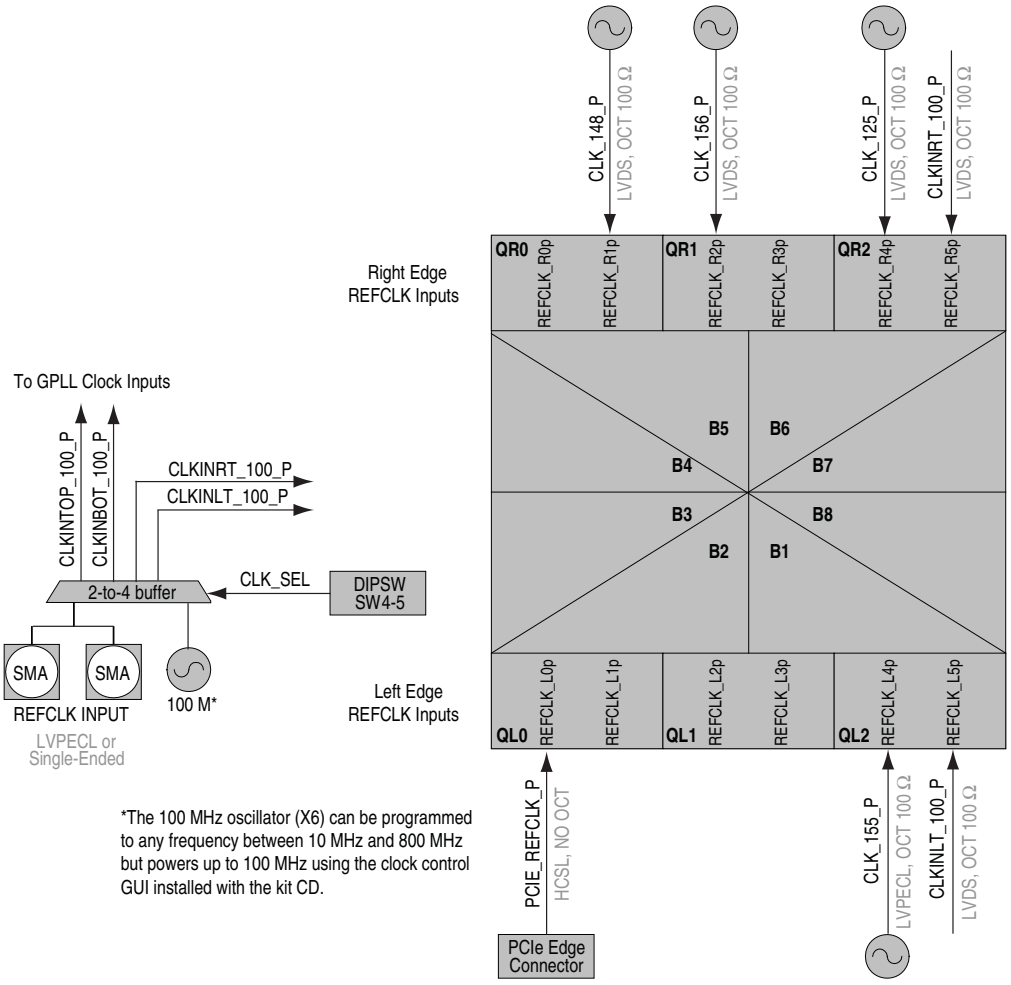


Table 2–20 lists the external clock inputs for the Stratix IV GX FPGA development board.

Table 2–20. Stratix IV GX FPGA Development Board Clock Inputs (Part 1 of 2)

Source	Schematic Signal Name	Pin	I/O Standard	Description
X1	CLK_125_P0	J2	LVDS	125 MHz oscillator which drives the transceiver reference clock input with 100 Ω on-chip termination (OCT).
	CLK_125_P1	AF34	LVDS	125 MHz oscillator which drives the global clock input with parallel OCT.
X2	CLK_156_P	AA2	LVDS	156.25 MHz oscillator which drives the transceiver reference clock input with 100 Ω OCT.
X3	CLK_148_P	AL2	LVDS	148.5 MHz oscillator which drives the transceiver reference clock input with 100 Ω OCT.

Table 2–20. Stratix IV GX FPGA Development Board Clock Inputs (Part 2 of 2)

Source	Schematic Signal Name	Pin	I/O Standard	Description
X7	CLK_155_P	J38	LVPECL	155.52 MHz oscillator which drives the transceiver reference clock input with 100 Ω OCT.
X8	CLKIN_50	AC34	2.5-V CMOS	50 MHz oscillator which drives the global clock input.
SMA or X6	CLKINTOP_100_P	A21	LVDS	100 MHz programmable oscillator which drives the fan-out buffer U50 and LVDS input to the top edge PLL input.
	CLKINTOP_100_N	A20		
	CLKINBOT_100_P	AV22	LVDS	100 MHz programmable oscillator which drives the fan-out buffer U50 and LVDS input to the top edge PLL input.
	CLKINBOT_100_N	AW22		
	CLKINRT_100_P	G2	LVDS	100 MHz programmable oscillator which drives the fan-out buffer U50 and LVDS to the transceiver QR2 REFCLK input.
	CLKINRT_100_N	G1		
	CLKINLT_100_P	G38	LVDS	100 MHz programmable oscillator which drives the fan-out buffer U50 and LVDS to the transceiver QR2 REFCLK input.
	CLKINLT_100_N	G39		
Samtec HSMC	HSMA_CLK_IN0	AB34	LVTTL	Single-ended input from the installed HSMC cable or board.
Samtec HSMC	HSMA_CLK_IN_P1	AC6	LVDS or LVTTL	LVDS input from the installed HSMC cable or board. Can also support two LVTTL inputs.
	HSMA_CLK_IN_N1	AC5		
Samtec HSMC	HSMA_CLK_IN_P2	AF6	LVDS or LVTTL	LVDS input from the installed HSMC cable or board. Can also support two LVTTL inputs.
	HSMA_CLK_IN_N2	AE5		
Samtec HSMC	HSMB_CLK_IN0	AA35	LVTTL	Single-ended input from the installed HSMC cable or board.
Samtec HSMC	HSMB_CLK_IN_P1	AB6	LVDS or LVTTL	LVDS input from the installed HSMC cable or board. Can also support two LVTTL inputs.
	HSMB_CLK_IN_N1	AA5		
Samtec HSMC	HSMB_CLK_IN_P2	W6	LVDS or LVTTL	LVDS input from the installed HSMC cable or board. Can also support two LVTTL inputs.
	HSMB_CLK_IN_N2	W5		
PCI Express Edge	PCIE_REFCLK_P	AN38	HCSL	HCSL input from the PCI Express edge connector.
	PCIE_REFCLK_N	AN39		

Stratix IV GX FPGA Clock Outputs

Figure 2–8 shows the Stratix IV GX FPGA development board clock outputs.

Figure 2–8. Stratix IV GX FPGA Development Board Clock Outputs

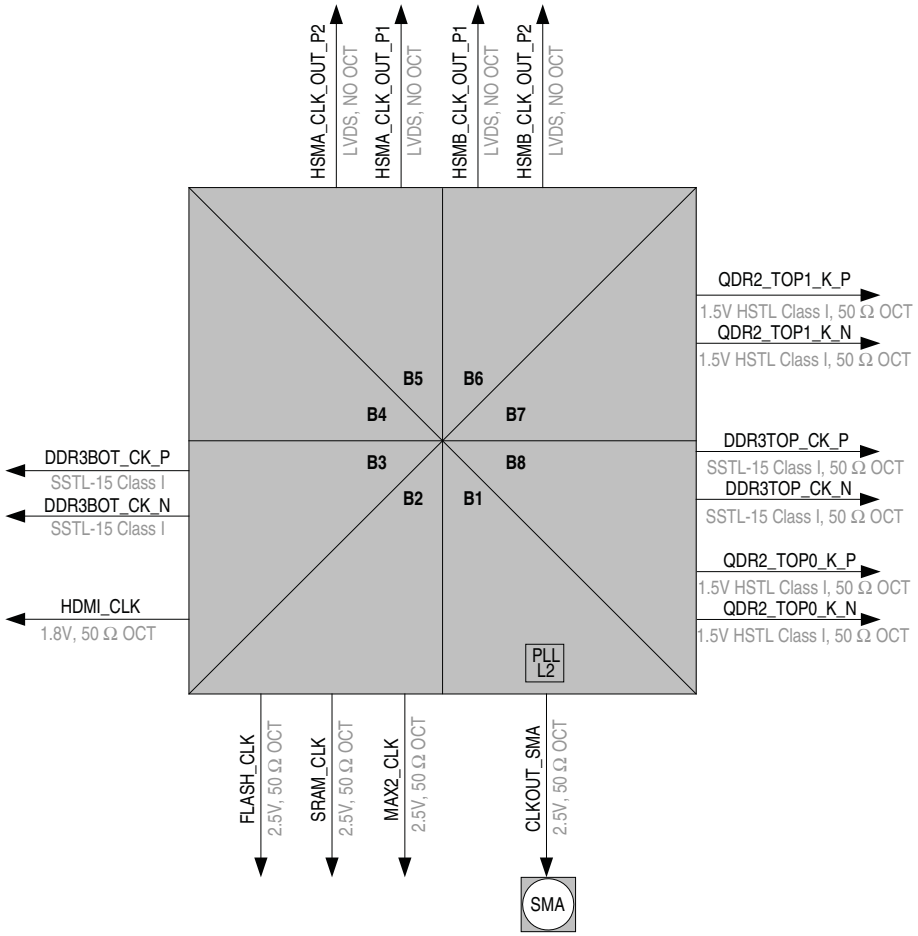


Table 2–21 lists the clock outputs for the Stratix IV GX FPGA development board.

Table 2–21. Stratix IV GX FPGA Development Board Clock Outputs (Part 1 of 2)

Connector	Schematic Signal Name	Pin	I/O Standard	Description
SMA	CLKOUT_SMA	W33	2.5-V	FPGA CMOS output or general purpose I/O (GPIO)
Samtec HSMC	HSMA_CLK_OUT0	AM29	2.5-V	FPGA CMOS output or GPIO
Samtec HSMC	HSMA_CLK_OUT_P1	AL10	LVDS or 2.5-V	LVDS output or two 2.5-V CMOS outputs.
	HSMA_CLK_OUT_N1	AM10		
Samtec HSMC	HSMA_CLK_OUT_P2	AF13	LVDS or 2.5-V	LVDS output or two 2.5-V CMOS outputs.
	HSMA_CLK_OUT_N2	AG13		
Samtec HSMC	HSMB_CLK_OUT0	AK29	2.5-V	FPGA CMOS output or GPIO
Samtec HSMC	HSMB_CLK_OUT_P1	K8	LVDS or 2.5-V	LVDS output or two 2.5-V CMOS outputs.
	HSMB_CLK_OUT_N1	J8		

Table 2–21. Stratix IV GX FPGA Development Board Clock Outputs (Part 2 of 2)

Connector	Schematic Signal Name	Pin	I/O Standard	Description
Samtec HSMC	HSMB_CLK_OUT_P2	K10	LVDS or 2.5-V	LVDS output. Can also support two CMOS outputs.
	HSMB_CLK_OUT_N3	J10		

Table 2–22 lists the crystal oscillators component references and manufacturing information.

Table 2–22. Crystal Oscillator Component References and Manufacturing Information (1)

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
X1	125 MHz LVDS Saw Oscillator	Epson	EG-2121CA 125.0000M-LGPNL3	www.eea.epson.com
X2	156.25 MHz LVDS Saw Oscillator	Epson	EG-2121CA 156.2500M-LHPNL3	www.eea.epson.com
X3	148.5 MHz Voltage Controlled LVDS Crystal Oscillator	Connor-Winfield	V902-148.5MHz	www.conwin.com
X6	100 MHz LVDS Programmable Crystal Oscillator	Silicon Labs	570FAB000433DG	www.silabs.com
X7	155.5 MHz LVPECL Saw Oscillator	Epson	EG-2121CA 155.5200M-PGPNL3	www.eea.epson.com
X8	50 MHz Crystal Oscillator	Epson	XG-1000CB 50.0000M-DCL3	www.eea.epson.com
X9	125 MHz Crystal Oscillator	ECS	ECS-3525-1250-B	www.ecsxtal.com

Note for Table 2–22:

(1) The crystal oscillator whose component reference and manufacturing information on the engineering silicon board differ from the production silicon board is listed in Table A–3 on page A–3.

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push buttons, DIP switches, status LEDs, and character LCD.

User-Defined Push Buttons

The development board includes four user-defined push buttons—three general and one CPU reset. For information on the system and safe reset push buttons, refer to "Reset Configuration Push Button" on page 2–20.

Board references S3, S4, and S5 are push buttons that allow you to interact with the Stratix IV GX device. When you press and hold down the push button, the device pin is set to logic 0; when you release the push button, the device pin is set to logic 1. There is no board-specific function for these general user push buttons.

Board reference S2 is the CPU reset push button, CPU_RESETn, which is an input to both the Stratix IV GX device and MAX II CPLD EPM2210 System Controller. The CPU_RESETn is the master reset signal for the FPGA design loaded into the Stratix IV GX device. The CPU_RESETn signal must be enabled within the Quartus II software for this reset function to work. Otherwise, the CPU_RESETn acts as a regular I/O pin. When enabled in the Quartus II software, and then pulled high on the board, this switch resets every register within the FPGA.

Table 2–23 lists the user-defined push button schematic signal names and their corresponding Stratix IV GX device pin numbers.

Table 2–23. User-Defined Push Button Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
S2	User-defined push button	CPU_RESETn	2.5-V	V34
S3		USER_PB2		M34
S4		USER_PB1		W32
S5		USER_PB0		AK35

Table 2–24 lists the user-defined push button component reference and the manufacturing information.

Table 2–24. User-Defined Push Button Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S2 to S5	Push button	Panasonic Corporation	EVQPAC07K	www.panasonic.com

User-Defined DIP Switch

Board reference S6 is an 8-pin DIP switch. This switch is user-defined and are provided for additional FPGA input control. There is no board-specific function for these switches.

Table 2–25 lists the user-defined DIP switch schematic signal names and their corresponding Stratix IV GX pin numbers.

Table 2–25. User-Defined DIP Switch Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
SW3.1	User-defined DIP switch that connects to the FPGA device. When the switch is in the OPEN or OFF position, a logic 1 is selected. When the switch is in the CLOSED or ON position, a logic 0 is selected.	USER_DIPSW0	2.5-V	AL35
SW3.2		USER_DIPSW1		AC35
SW3.3		USER_DIPSW2		J34
SW3.4		USER_DIPSW3		AN35
SW3.5		USER_DIPSW4		G33
SW3.6		USER_DIPSW5		K35
SW3.7		USER_DIPSW6		AG34
SW3.8		USER_DIPSW7		AG31

Table 2–26 lists the user-defined DIP switch component reference and the manufacturing information.

Table 2–26. User-Defined DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW3	Eight-position DIP switch	C & K Components	TDA08H0SB1	www.ck-components.com

User-Defined LEDs

The development board includes general and HSMC user-defined LEDs. This section describes all user-defined LEDs. For information on board specific or status LEDs, refer to"Status Elements" on page 2–17.

General User-Defined LEDs

Board references D6 through D13 and D16 through D23 are 16 user LEDs that allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix IV GX device. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

Table 2–27 lists the user-defined LED schematic signal names and their corresponding Stratix IV GX pin numbers.

Table 2–27. User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
D23	User-defined LEDs. Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	USR_LED0	2.5-V	F33
D22		USR_LED1	2.5-V	AK33
D21		USR_LED2	2.5-V	W28
D20		USR_LED3	2.5-V	L34
D19		USR_LED4	2.5-V	AM34
D18		USR_LED5	2.5-V	M32
D17		USR_LED6	2.5-V	L35
D16		USR_LED7	2.5-V	AM35
D13		USR_LED8	2.5-V	N34
D12		USR_LED9	2.5-V	W35
D11		USR_LED10	2.5-V	AE30
D10		USR_LED11	2.5-V	V30
D9		USR_LED12	2.5-V	AG30
D8		USR_LED13	2.5-V	AD29
D7		USR_LED14	2.5-V	U31
D6		USR_LED15	2.5-V	U35

Table 2–28 lists the user-defined LED component reference and the manufacturing information.

Table 2–28. User-Defined LED Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D6 to D13, D16 to D23	Green LEDs, 1206, SMT, Clear Lens, 2.1 V	Lumex Inc.	SML-LX1206GC-TR	www.lumex.com

HSMC User-Defined LEDs

The HSMC port A and B have two LEDs located nearby. There are no board-specific functions for the HSMC LEDs. However, the LEDs are labeled TX and RX, and are intended to display data flow to and from the connected HSMC cards. The LEDs are driven by the Stratix IV GX device.

Table 2–29 lists the HSMC user-defined LED schematic signal names and their corresponding Stratix IV GX pin numbers.

Table 2–29. HSMC User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
D3	User-Defined LEDs. Labeled TX for HSMC Port A.	HSMA_TX_LED	2.5-V	D5
D4	User-Defined LEDs. Labeled RX for HSMC Port A.	HSMA_RX_LED		C6
D14	User-Defined LEDs. Labeled TX for HSMC Port B.	HSMB_TX_LED		AH33
D15	User-Defined LEDs. Labeled RX for HSMC Port B.	HSMB_RX_LED		AT10

Table 2–30 lists the HSMC user-defined LED component reference and the manufacturing information.

Table 2–30. HSMC User-Defined LED Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D3 to D4 D14 to D15	Green LEDs, 1206, SMT, Clear Lens, 2.1 V	Lumex Inc.	SML-LX1206GC-TR	www.lumex.com

LCD

The development board contains a single 14-pin 0.1" pitch dual-row header that interfaces to a 16 character × 2 line Lumex LCD display. The LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

Table 2–31 summarizes the LCD pin assignments. The signal names and directions are relative to the Stratix IV GX FPGA.

Table 2–31. LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J16.7	LCD data bus	LCD_DATA0	2.5-V	AD31
J16.8	LCD data bus	LCD_DATA1	2.5-V	AJ34
J16.9	LCD data bus	LCD_DATA2	2.5-V	R31
J16.10	LCD data bus	LCD_DATA3	2.5-V	L32
J16.11	LCD data bus	LCD_DATA4	2.5-V	T30
J16.12	LCD data bus	LCD_DATA5	2.5-V	AN34
J16.13	LCD data bus	LCD_DATA6	2.5-V	T31
J16.14	LCD data bus	LCD_DATA7	2.5-V	AD30
J16.4	LCD data or command select	LCD_D_Cn	2.5-V	AB30
J16.5	LCD write enable	LCD_Wen	2.5-V	AL34
J16.6	LCD chip select	LCD_CSn	2.5-V	K34

Table 2–32 shows the LCD pin definitions, and is an excerpt from the Lumex data sheet.

For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

Table 2–32. LCD Pin Definitions and Functions

Pin Number	Symbol	Level	Function	
1	V_{DD}	—	Power supply	5 V
2	V_{SS}	—		GND (0 V)
3	V_0	—		For LCD drive
4	RS	H/L	Register select signal H: Data input L: Instruction input	
5	R/W	H/L	H: Data read (module to MPU) L: Data write (MPU to module)	
6	E	H, H to L	Enable	
7–14	DB0–DB7	H/L	Data bus, software selectable 4-bit or 8-bit mode	

The particular model on this board does not have a backlight and the LCD drive pin is not connected.

Table 2–33 lists the LCD component references and the manufacturing information.

Table 2–33. LCD Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J16	2×7 pin, 100 mil, vertical header	Samtec	TSM-107-01-G-DV	www.samtec.com
	2×16 character display, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com

Components and Interfaces

This section describes the development board communication ports and interface cards relative to the Stratix IV GX device. The development board supports the following communication ports:

- PCI Express
- 10/100/1000 Ethernet
- HSMC

PCI Express

The Stratix IV GX FPGA development board is designed to fit entirely into a PC motherboard with a ×8 or ×16 PCI Express slot that can accommodate a full height short form factor add-in card. This interface uses the Stratix IV GX device's PCI Express hard IP block, saving logic resources for the user logic application.

For more information on using the PCI Express hard IP block, refer to the *PCI Express Compiler User Guide*.

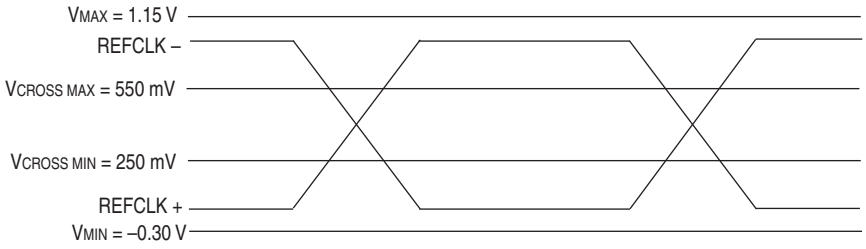
The PCI Express interface supports auto-negotiating channel width from ×1 to ×4 to ×8 as well as the connection speed of Gen1 at 2.5 Gbps/lane to Gen2 at 5.0 Gbps/lane for a maximum of 40 Gbps full-duplex. The PCI Express control DIP switch allows the presence detect grounding to be altered to enable a ×1, ×4, or ×8 width edge connector.

The power for the board can be sourced entirely from the PCI Express edge connector when installed into a PC motherboard. Although the board can also be powered by a laptop power supply for use on a lab bench, it is not recommended to power from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The `PCIE_REFCLK_P` signal is a 100-MHz differential input that is driven from the PC motherboard on this board through the edge connector. This signal is connected directly to a Stratix IV GX `REFCLK` input pin pair using DC coupling. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL).

Figure 2–9 shows the PCI Express reference clock levels.

Figure 2–9. PCI Express Reference Clock Levels



The JTAG and SMB are optional signals in the PCI Express specification. Both types of signals are wired to the Stratix IV GX device but are not required for normal operation. Table 2–34 lists the PCI Express pin assignments. The signal names and directions are relative to the Stratix IV GX FPGA.

Table 2–34. PCI Express Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J17.A47	Add-in card transmit bus	PCIE_TX_P7	1.4-V PCML	P36
J17.A48	Add-in card transmit bus	PCIE_TX_N7	1.4-V PCML	P37
J17.A43	Add-in card transmit bus	PCIE_TX_P6	1.4-V PCML	T36
J17.A44	Add-in card transmit bus	PCIE_TX_N6	1.4-V PCML	T37
J17.A39	Add-in card transmit bus	PCIE_TX_P5	1.4-V PCML	AB36
J17.A40	Add-in card transmit bus	PCIE_TX_N5	1.4-V PCML	AB37
J17.A35	Add-in card transmit bus	PCIE_TX_P4	1.4-V PCML	AD36
J17.A36	Add-in card transmit bus	PCIE_TX_N4	1.4-V PCML	AD37
J17.A29	Add-in card transmit bus	PCIE_TX_P3	1.4-V PCML	AF36
J17.A30	Add-in card transmit bus	PCIE_TX_N3	1.4-V PCML	AF37
J17.A25	Add-in card transmit bus	PCIE_TX_P2	1.4-V PCML	AH36
J17.A26	Add-in card transmit bus	PCIE_TX_N2	1.4-V PCML	AH37
J17.A21	Add-in card transmit bus	PCIE_TX_P1	1.4-V PCML	AP36
J17.A22	Add-in card transmit bus	PCIE_TX_N1	1.4-V PCML	AP37
J17.A16	Add-in card transmit bus	PCIE_TX_P0	1.4-V PCML	AT36
J17.A17	Add-in card transmit bus	PCIE_TX_N0	1.4-V PCML	AT37
J17.B45	Add-in card receive bus	PCIE_RX_P7	1.4-V PCML	R38
J17.B46	Add-in card receive bus	PCIE_RX_N7	1.4-V PCML	R39
J17.B41	Add-in card receive bus	PCIE_RX_P6	1.4-V PCML	U38
J17.B42	Add-in card receive bus	PCIE_RX_N6	1.4-V PCML	U39
J17.B37	Add-in card receive bus	PCIE_RX_P5	1.4-V PCML	AC38
J17.B38	Add-in card receive bus	PCIE_RX_N5	1.4-V PCML	AC39
J17.B33	Add-in card receive bus	PCIE_RX_P4	1.4-V PCML	AE38
J17.B34	Add-in card receive bus	PCIE_RX_N4	1.4-V PCML	AE39

Table 2–34. PCI Express Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J17.B27	Add-in card receive bus	PCIE_RX_P3	1.4-V PCML	AG38
J17.B28	Add-in card receive bus	PCIE_RX_N3	1.4-V PCML	AG39
J17.B23	Add-in card receive bus	PCIE_RX_P2	1.4-V PCML	AJ38
J17.B24	Add-in card receive bus	PCIE_RX_N2	1.4-V PCML	AJ39
J17.B19	Add-in card receive bus	PCIE_RX_P1	1.4-V PCML	AR38
J17.B20	Add-in card receive bus	PCIE_RX_N1	1.4-V PCML	AR39
J17.B14	Add-in card receive bus	PCIE_RX_P0	1.4-V PCML	AU38
J17.B15	Add-in card receive bus	PCIE_RX_N0	1.4-V PCML	AU39
J17.A13	Motherboard reference clock	PCIE_REFCLK_P	HCSL	AN38
J17.A14	Motherboard reference clock	PCIE_REFCLK_N	HCSL	AN39
J17.A11	Reset	PCIE_PERSTn	LVTTL	R32
J17.B11	Wake signal	PCIE_WAKEn	LVTTL	P31
J17.B5	SMB clock	PCIE_SMBCLK	LVTTL	AE31
J17.B6	SMB data	PCIE_SMBDAT	LVTTL	P32

10/100/1000 Ethernet

A Marvell 88E1111 PHY device is used for 10/100/1000 BASE-T Ethernet connection. The device is an auto-negotiating Ethernet PHY with an SGMII interface to the FPGA. The Stratix IV GX device can communicate with the LVDS interfaces at up to 1.6 Gbps, which is faster than 1.25 Gbps for SGMII. The MAC function must be provided in the FPGA for typical networking applications. The Marvell 88E1111 PHY uses 2.5-V and 1.1-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. It interfaces to an RJ-45 with internal magnetics for driving copper lines with Ethernet traffic.

Figure 2–10 shows the SGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2–10. SGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

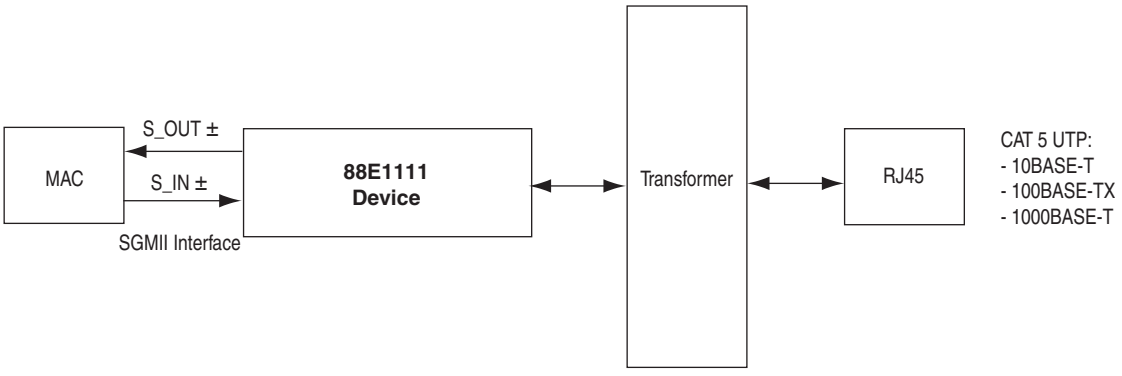


Table 2–35 lists the Ethernet PHY interface pin assignments.

Table 2–35. Ethernet PHY Pin Assignments, Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U21.82	SGMII TX data	ENET_TX_P	LVDS	L29
U21.81	SGMII TX data	ENET_TX_N		K29
U21.77	SGMII RX data	ENET_RX_P		AC31
U21.75	SGMII RX data	ENET_RX_N		AC32
U21.25	Management bus control	ENET_MDC	2.5-V	AH34
U21.24	Management bus data	ENET_MDIO		M33
U21.23	Management bus interrupt	ENET_INTn		R30
U21.28	Device reset	ENET_RESETn		V31

Table 2–36 lists the Ethernet PHY interface component reference and manufacturing information.

Table 2–36. Ethernet PHY Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U21	Ethernet PHY BASE-T device	Marvel Semiconductor	88E1111-B2-CAAIC000	www.marvell.com

HSMC

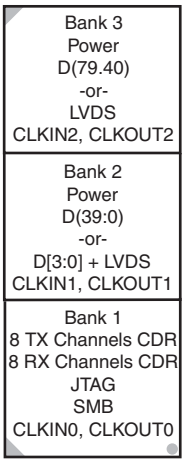
The development board contains two HSMC interfaces, port A and port B. These HSMC interfaces support both single-ended and differential signaling. The HSMC interface also allows JTAG, SMB, clock outputs and inputs, as well as power for compatible HSMC cards. The HSMC is an Altera-developed open specification, which allows you to expand the functionality of the development board through the addition of daughtercards.

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 2–11 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

Figure 2–11. HSMC Signal and Bank Diagram



The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

☞ As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–37 lists the HSMC port A interface pin assignments, signal names, and functions.

Table 2–37. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J1.1	Transceiver TX bit 7	HSMA_TX_P7	1.4-V PCML	P4
J1.2	Transceiver RX bit 7	HSMA_RX_P7	1.4-V PCML	R2
J1.3	Transceiver TX bit 7n	HSMA_TX_N7	1.4-V PCML	P3
J1.4	Transceiver RX bit 7n	HSMA_RX_N7	1.4-V PCML	R1
J1.5	Transceiver TX bit 6	HSMA_TX_P6	1.4-V PCML	T4
J1.6	Transceiver RX bit 6	HSMA_RX_P6	1.4-V PCML	U2
J1.7	Transceiver TX bit 6n	HSMA_TX_N6	1.4-V PCML	T3
J1.8	Transceiver RX bit 6n	HSMA_RX_N6	1.4-V PCML	U1
J1.9	Transceiver TX bit 5	HSMA_TX_P5	1.4-V PCML	AB4
J1.10	Transceiver RX bit 5	HSMA_RX_P5	1.4-V PCML	AC2
J1.11	Transceiver TX bit 5n	HSMA_TX_N5	1.4-V PCML	AB3
J1.12	Transceiver RX bit 5n	HSMA_RX_N5	1.4-V PCML	AC1

Table 2–37. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J1.13	Transceiver TX bit 4	HSMA_TX_P4	1.4-V PCML	AD4
J1.14	Transceiver RX bit 4	HSMA_RX_P4	1.4-V PCML	AE2
J1.15	Transceiver TX bit 4n	HSMA_TX_N4	1.4-V PCML	AD3
J1.16	Transceiver RX bit 4n	HSMA_RX_N4	1.4-V PCML	AE1
J1.17	Transceiver TX bit 3	HSMA_TX_P3	1.4-V PCML	AF4
J1.18	Transceiver RX bit 3	HSMA_RX_P3	1.4-V PCML	AG2
J1.19	Transceiver TX bit 3n	HSMA_TX_N3	1.4-V PCML	AF3
J1.20	Transceiver RX bit 3n	HSMA_RX_N3	1.4-V PCML	AG1
J1.21	Transceiver TX bit 2	HSMA_TX_P2	1.4-V PCML	AH4
J1.22	Transceiver RX bit 2	HSMA_RX_P2	1.4-V PCML	AJ2
J1.23	Transceiver TX bit 2n	HSMA_TX_N2	1.4-V PCML	AH3
J1.24	Transceiver RX bit 2n	HSMA_RX_N2	1.4-V PCML	AJ1
J1.25	Transceiver TX bit 1	HSMA_TX_P1	1.4-V PCML	AP4
J1.26	Transceiver RX bit 1	HSMA_RX_P1	1.4-V PCML	AR2
J1.27	Transceiver TX bit 1n	HSMA_TX_N1	1.4-V PCML	AP3
J1.28	Transceiver RX bit 1n	HSMA_RX_N1	1.4-V PCML	AR1
J1.29	Transceiver TX bit 0	HSMA_TX_P0	1.4-V PCML	AT4
J1.30	Transceiver RX bit 0	HSMA_RX_P0	1.4-V PCML	AU2
J1.31	Transceiver TX bit 0n	HSMA_TX_N0	1.4-V PCML	AT3
J1.32	Transceiver RX bit 0n	HSMA_RX_N0	1.4-V PCML	AU1
J1.33	Management serial data	HSMA_SDA	2.5-V	AJ11
J1.34	Management serial clock	HSMA_SCL		L11
J1.35	JTAG clock signal	FPGA_JTAG_TCK	2.5-V	—
J1.36	JTAG mode select signal	FPGA_JTAG_TMS	2.5-V	—
J1.37	JTAG data output	HSMA_JTAG_TDO	2.5-V	—
J1.38	JTAG data input	HSMA_JTAG_TDI	2.5-V	—
J1.39	Dedicated CMOS clock out	HSMA_CLK_OUT0	2.5-V	AM29
J1.40	Dedicated CMOS clock in	HSMA_CLK_IN0	2.5-V	AB34
J1.41	Dedicated CMOS I/O bit 0	HSMA_D0	2.5-V	AW10
J1.42	Dedicated CMOS I/O bit 1	HSMA_D1	2.5-V	AV10
J1.43	Dedicated CMOS I/O bit 2	HSMA_D2	2.5-V	AW7
J1.44	Dedicated CMOS I/O bit 3	HSMA_D3	2.5-V	AV7
J1.47	LVDS TX bit 0 or CMOS bit 4	HSMA_TX_D_P0	LVDS or 2.5-V	AN9
J1.48	LVDS RX bit 0 or CMOS bit 5	HSMA_RX_D_P0	LVDS or 2.5-V	AT9
J1.49	LVDS TX bit 0n or CMOS bit 6	HSMA_TX_D_N0	LVDS or 2.5-V	AP9
J1.50	LVDS RX bit 0n or CMOS bit 7	HSMA_RX_D_N0	LVDS or 2.5-V	AU9
J1.53	LVDS TX bit 1 or CMOS bit 8	HSMA_TX_D_P1	LVDS or 2.5-V	AN7
J1.54	LVDS RX bit 1 or CMOS bit 9	HSMA_RX_D_P1	LVDS or 2.5-V	AT8

Table 2–37. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J1.55	LVDS TX bit 1n or CMOS bit 10	HSMA_TX_D_N1	LVDS or 2.5-V	AP7
J1.56	LVDS RX bit 1n or CMOS bit 11	HSMA_RX_D_N1	LVDS or 2.5-V	AU8
J1.59	LVDS TX bit 2 or CMOS bit 12	HSMA_TX_D_P2	LVDS or 2.5-V	AE13
J1.60	LVDS RX bit 2 or CMOS bit 13	HSMA_RX_D_P2	LVDS or 2.5-V	AP8
J1.61	LVDS TX bit 2n or CMOS bit 14	HSMA_TX_D_N2	LVDS or 2.5-V	AE12
J1.62	LVDS RX bit 2n or CMOS bit 15	HSMA_RX_D_N2	LVDS or 2.5-V	AR8
J1.65	LVDS TX bit 3 or CMOS bit 16	HSMA_TX_D_P3	LVDS or 2.5-V	AL8
J1.66	LVDS RX bit 3 or CMOS bit 17	HSMA_RX_D_P3	LVDS or 2.5-V	AW6
J1.67	LVDS TX bit 3n or CMOS bit 18	HSMA_TX_D_N3	LVDS or 2.5-V	AM8
J1.68	LVDS RX bit 3n or CMOS bit 19	HSMA_RX_D_N3	LVDS or 2.5-V	AW5
J1.71	LVDS TX bit 4 or CMOS bit 20	HSMA_TX_D_P4	LVDS or 2.5-V	AK9
J1.72	LVDS RX bit 4 or CMOS bit 21	HSMA_RX_D_P4	LVDS or 2.5-V	AV5
J1.73	LVDS TX bit 4n or CMOS bit 22	HSMA_TX_D_N4	LVDS or 2.5-V	AL9
J1.74	LVDS RX bit 4n or CMOS bit 23	HSMA_RX_D_N4	LVDS or 2.5-V	AW4
J1.77	LVDS TX bit 5 or CMOS bit 24	HSMA_TX_D_P5	LVDS or 2.5-V	AK8
J1.78	LVDS RX bit 5 or CMOS bit 25	HSMA_RX_D_P5	LVDS or 2.5-V	AT7
J1.79	LVDS TX bit 5n or CMOS bit 26	HSMA_TX_D_N5	LVDS or 2.5-V	AK7
J1.80	LVDS RX bit 5n or CMOS bit 27	HSMA_RX_D_N5	LVDS or 2.5-V	AU7
J1.83	LVDS TX bit 6 or CMOS bit 28	HSMA_TX_D_P6	LVDS or 2.5-V	AH10
J1.84	LVDS RX bit 6 or CMOS bit 29	HSMA_RX_D_P6	LVDS or 2.5-V	AT6
J1.85	LVDS TX bit 6n or CMOS bit 30	HSMA_TX_D_N6	LVDS or 2.5-V	AJ10
J1.86	LVDS RX bit 6n or CMOS bit 31	HSMA_RX_D_N6	LVDS or 2.5-V	AU6
J1.89	LVDS TX bit 7 or CMOS bit 32	HSMA_TX_D_P7	LVDS or 2.5-V	AH9
J1.90	LVDS RX bit 7 or CMOS bit 33	HSMA_RX_D_P7	LVDS or 2.5-V	AR5
J1.91	LVDS TX bit 7n or CMOS bit 34	HSMA_TX_D_N7	LVDS or 2.5-V	AH8
J1.92	LVDS RX bit 7n or CMOS bit 35	HSMA_RX_D_N7	LVDS or 2.5-V	AT5
J1.95	LVDS or CMOS clock out 1 or CMOS bit 36	HSMA_CLK_OUT_P1	LVDS or 2.5-V	AL10
J1.96	LVDS or CMOS clock in 1 or CMOS bit 37	HSMA_CLK_IN_P1	LVDS or 2.5-V	AC6
J1.97	LVDS or CMOS clock out 1 or CMOS bit 38	HSMA_CLK_OUT_N1	LVDS or 2.5-V	AM10
J1.98	LVDS or CMOS clock in 1 or CMOS bit 39	HSMA_CLK_IN_N1	LVDS or 2.5-V	AC5
J1.101	LVDS TX bit 8 or CMOS bit 40	HSMA_TX_D_P8	LVDS or 2.5-V	AG8
J1.102	LVDS RX bit 8 or CMOS bit 41	HSMA_RX_D_P8	LVDS or 2.5-V	AP6
J1.103	LVDS TX bit 8n or CMOS bit 42	HSMA_TX_D_N8	LVDS or 2.5-V	AG7
J1.104	LVDS RX bit 8n or CMOS bit 43	HSMA_RX_D_N8	LVDS or 2.5-V	AP5
J1.107	LVDS TX bit 9 or CMOS bit 44	HSMA_TX_D_P9	LVDS or 2.5-V	AG10
J1.108	LVDS RX bit 9 or CMOS bit 45	HSMA_RX_D_P9	LVDS or 2.5-V	AN6
J1.109	LVDS TX bit 9n or CMOS bit 46	HSMA_TX_D_N9	LVDS or 2.5-V	AG9
J1.110	LVDS RX bit 9n or CMOS bit 47	HSMA_RX_D_N9	LVDS or 2.5-V	AN5

Table 2–37. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J1.113	LVDS TX bit 10 or CMOS bit 48	HSMA_TX_D_P10	LVDS or 2.5-V	AF11
J1.114	LVDS RX bit 10 or CMOS bit 49	HSMA_RX_D_P10	LVDS or 2.5-V	AM6
J1.115	LVDS TX bit 10n or CMOS bit 50	HSMA_TX_D_N10	LVDS or 2.5-V	AF10
J1.116	LVDS RX bit 10n or CMOS bit 51	HSMA_RX_D_N10	LVDS or 2.5-V	AM5
J1.119	LVDS TX bit 11 or CMOS bit 52	HSMA_TX_D_P11	LVDS or 2.5-V	AD10
J1.120	LVDS RX bit 11 or CMOS bit 53	HSMA_RX_D_P11	LVDS or 2.5-V	AL6
J1.121	LVDS TX bit 11n or CMOS bit 54	HSMA_TX_D_N11	LVDS or 2.5-V	AD9
J1.122	LVDS RX bit 11n or CMOS bit 55	HSMA_RX_D_N11	LVDS or 2.5-V	AL5
J1.125	LVDS TX bit 12 or CMOS bit 56	HSMA_TX_D_P12	LVDS or 2.5-V	AE11
J1.126	LVDS RX bit 12 or CMOS bit 57	HSMA_RX_D_P12	LVDS or 2.5-V	AK6
J1.127	LVDS TX bit 12n or CMOS bit 58	HSMA_TX_D_N12	LVDS or 2.5-V	AE10
J1.128	LVDS RX bit 12n or CMOS bit 59	HSMA_RX_D_N12	LVDS or 2.5-V	AK5
J1.131	LVDS TX bit 13 or CMOS bit 60	HSMA_TX_D_P13	LVDS or 2.5-V	AD13
J1.132	LVDS RX bit 13 or CMOS bit 61	HSMA_RX_D_P13	LVDS or 2.5-V	AJ6
J1.133	LVDS TX bit 13n or CMOS bit 62	HSMA_TX_D_N13	LVDS or 2.5-V	AD12
J1.134	LVDS RX bit 13n or CMOS bit 63	HSMA_RX_D_N13	LVDS or 2.5-V	AJ5
J1.137	LVDS TX bit 14 or CMOS bit 64	HSMA_TX_D_P14	LVDS or 2.5-V	AB13
J1.138	LVDS RX bit 14 or CMOS bit 65	HSMA_RX_D_P14	LVDS or 2.5-V	AH6
J1.139	LVDS TX bit 14n or CMOS bit 66	HSMA_TX_D_N14	LVDS or 2.5-V	AB12
J1.140	LVDS RX bit 14n or CMOS bit 67	HSMA_RX_D_N14	LVDS or 2.5-V	AH5
J1.143	LVDS TX bit 15 or CMOS bit 68	HSMA_TX_D_P15	LVDS or 2.5-V	AB11
J1.144	LVDS RX bit 15 or CMOS bit 69	HSMA_RX_D_P15	LVDS or 2.5-V	AG6
J1.145	LVDS TX bit 15n or CMOS bit 70	HSMA_TX_D_N15	LVDS or 2.5-V	AB10
J1.146	LVDS RX bit 15n or CMOS bit 71	HSMA_RX_D_N15	LVDS or 2.5-V	AG5
J1.149	LVDS TX bit 16 or CMOS bit 72	HSMA_TX_D_P16	LVDS or 2.5-V	AC11
J1.150	LVDS RX bit 16 or CMOS bit 73	HSMA_RX_D_P16	LVDS or 2.5-V	AB9
J1.151	LVDS TX bit 16n or CMOS bit 74	HSMA_TX_D_N16	LVDS or 2.5-V	AC10
J1.152	LVDS RX bit 16n or CMOS bit 75	HSMA_RX_D_N16	LVDS or 2.5-V	AC8
J1.155	LVDS or CMOS clock out 2 or CMOS bit 76	HSMA_CLK_OUT_P2	LVDS or 2.5-V	AF13
J1.156	LVDS or CMOS clock in 2 or CMOS bit 77	HSMA_CLK_IN_P2	LVDS or 2.5-V	AF6
J1.157	LVDS or CMOS clock out 2 or CMOS bit 78	HSMA_CLK_OUT_N2	LVDS or 2.5-V	AG13
J1.158	LVDS or CMOS clock in 2 or CMOS bit 79	HSMA_CLK_IN_N2	LVDS or 2.5-V	AE5
J1.160	HSMC Port A presence detect	HSMA_PRSNTn	2.5-V	AG12
D4	User LED to show RX data activity on HSMC Port A	HSMA_RX_LED	2.5-V	D5
D3	User LED to show TX data activity on HSMC Port A	HSMA_TX_LED	2.5-V	C6

Table 2–38 lists the HSMC port B interface pin assignments, signal names, and functions.

Table 2–38. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J2.1	Transceiver TX bit 7	HSMB_TX_P7	1.4-V PCML	—
J2.2	Transceiver RX bit 7	HSMB_RX_P7	1.4-V PCML	—
J2.3	Transceiver TX bit 7n	HSMB_TX_N7	1.4-V PCML	—
J2.4	Transceiver RX bit 7n	HSMB_RX_N7	1.4-V PCML	—
J2.5	Transceiver TX bit 6	HSMB_TX_P6	1.4-V PCML	—
J2.6	Transceiver RX bit 6	HSMB_RX_P6	1.4-V PCML	—
J2.7	Transceiver TX bit 6n	HSMB_TX_N6	1.4-V PCML	—
J2.8	Transceiver RX bit 6n	HSMB_RX_N6	1.4-V PCML	—
J2.9	Transceiver TX bit 5	HSMB_TX_P5	1.4-V PCML	D4
J2.10	Transceiver RX bit 5	HSMB_RX_P5	1.4-V PCML	E2
J2.11	Transceiver TX bit 5n	HSMB_TX_N5	1.4-V PCML	D3
J2.12	Transceiver RX bit 5n	HSMB_RX_N5	1.4-V PCML	E1
J2.13	Transceiver TX bit 4	HSMB_TX_P4	1.4-V PCML	B4
J2.14	Transceiver RX bit 4	HSMB_RX_P4	1.4-V PCML	C2
J2.15	Transceiver TX bit 4n	HSMB_TX_N4	1.4-V PCML	B3
J2.16	Transceiver RX bit 4n	HSMB_RX_N4	1.4-V PCML	C1
J2.17	Transceiver TX bit 3	HSMB_TX_P3	1.4-V PCML	B36
J2.18	Transceiver RX bit 3	HSMB_RX_P3	1.4-V PCML	C38
J2.19	Transceiver TX bit 3n	HSMB_TX_N3	1.4-V PCML	B37
J2.20	Transceiver RX bit 3n	HSMB_RX_N3	1.4-V PCML	C39
J2.21	Transceiver TX bit 2	HSMB_TX_P2	1.4-V PCML	D36
J2.22	Transceiver RX bit 2	HSMB_RX_P2	1.4-V PCML	E38
J2.23	Transceiver TX bit 2n	HSMB_TX_N2	1.4-V PCML	D37
J2.24	Transceiver RX bit 2n	HSMB_RX_N2	1.4-V PCML	E39
J2.25	Transceiver TX bit 1	HSMB_TX_P1	1.4-V PCML	K36
J2.26	Transceiver RX bit 1	HSMB_RX_P1	1.4-V PCML	L38
J2.27	Transceiver TX bit 1n	HSMB_TX_N1	1.4-V PCML	K37
J2.28	Transceiver RX bit 1n	HSMB_RX_N1	1.4-V PCML	L39
J2.29	Transceiver TX bit 0	HSMB_TX_P0	1.4-V PCML	M36
J2.30	Transceiver RX bit 0	HSMB_RX_P0	1.4-V PCML	N38
J2.31	Transceiver TX bit 0n	HSMB_TX_N0	1.4-V PCML	M37
J2.32	Transceiver RX bit 0n	HSMB_RX_N0	1.4-V PCML	N39
J2.33	Management serial data	HSMB_SDA	2.5-V	AF29
J2.34	Management serial clock	HSMB_SCL	2.5-V	AB27
J2.35	JTAG clock signal	FPGA_JTAG_TCK	2.5-V	—
J2.36	JTAG mode select signal	FPGA_JTAG_TMS	2.5-V	—

Table 2–38. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J2.37	JTAG data output	HSMB_JTAG_TDO	2.5-V	—
J2.38	JTAG data input	HSMB_JTAG_TDI	2.5-V	—
J2.39	Dedicated CMOS clock out	HSMB_CLK_OUT0	2.5-V	AK29
J2.40	Dedicated CMOS clock in	HSMB_CLK_IN0	2.5-V	AA35
J2.41	Dedicated CMOS I/O bit 0	HSMB_D0	2.5-V	AP10
J2.42	Dedicated CMOS I/O bit 1	HSMB_D1	2.5-V	AN10
J2.43	Dedicated CMOS I/O bit 2	HSMB_D2	2.5-V	AW8
J2.44	Dedicated CMOS I/O bit 3	HSMB_D3	2.5-V	AV8
J2.47	LVDS TX bit 0 or CMOS bit 4	HSMB_TX_D_P0	LVDS or 2.5-V	W12
J2.48	LVDS RX bit 0 or CMOS bit 5	HSMB_RX_D_P0	LVDS or 2.5-V	W8
J2.49	LVDS TX bit 0n or CMOS bit 6	HSMB_TX_D_N0	LVDS or 2.5-V	W11
J2.50	LVDS RX bit 0n or CMOS bit 7	HSMB_RX_D_N0	LVDS or 2.5-V	W7
J2.53	LVDS TX bit 1 or CMOS bit 8	HSMB_TX_D_P1	LVDS or 2.5-V	V12
J2.54	LVDS RX bit 1 or CMOS bit 9	HSMB_RX_D_P1	LVDS or 2.5-V	V6
J2.55	LVDS TX bit 1n or CMOS bit 10	HSMB_TX_D_N1	LVDS or 2.5-V	V11
J2.56	LVDS RX bit 1n or CMOS bit 11	HSMB_RX_D_N1	LVDS or 2.5-V	U5
J2.59	LVDS TX bit 2 or CMOS bit 12	HSMB_TX_D_P2	LVDS or 2.5-V	V10
J2.60	LVDS RX bit 2 or CMOS bit 13	HSMB_RX_D_P2	LVDS or 2.5-V	R7
J2.61	LVDS TX bit 2n or CMOS bit 14	HSMB_TX_D_N2	LVDS or 2.5-V	V9
J2.62	LVDS RX bit 2n or CMOS bit 15	HSMB_RX_D_N2	LVDS or 2.5-V	P6
J2.65	LVDS TX bit 3 or CMOS bit 16	HSMB_TX_D_P3	LVDS or 2.5-V	U10
J2.66	LVDS RX bit 3 or CMOS bit 17	HSMB_RX_D_P3	LVDS or 2.5-V	R6
J2.67	LVDS TX bit 3n or CMOS bit 18	HSMB_TX_D_N3	LVDS or 2.5-V	T9
J2.68	LVDS RX bit 3n or CMOS bit 19	HSMB_RX_D_N3	LVDS or 2.5-V	R5
J2.71	LVDS TX bit 4 or CMOS bit 20	HSMB_TX_D_P4	LVDS or 2.5-V	T10
J2.72	LVDS RX bit 4 or CMOS bit 21	HSMB_RX_D_P4	LVDS or 2.5-V	N6
J2.73	LVDS TX bit 4n or CMOS bit 22	HSMB_TX_D_N4	LVDS or 2.5-V	R10
J2.74	LVDS RX bit 4n or CMOS bit 23	HSMB_RX_D_N4	LVDS or 2.5-V	N5
J2.77	LVDS TX bit 5 or CMOS bit 24	HSMB_TX_D_P5	LVDS or 2.5-V	R9
J2.78	LVDS RX bit 5 or CMOS bit 25	HSMB_RX_D_P5	LVDS or 2.5-V	N8
J2.79	LVDS TX bit 5n or CMOS bit 26	HSMB_TX_D_N5	LVDS or 2.5-V	R8
J2.80	LVDS RX bit 5n or CMOS bit 27	HSMB_RX_D_N5	LVDS or 2.5-V	N7
J2.83	LVDS TX bit 6 or CMOS bit 28	HSMB_TX_D_P6	LVDS or 2.5-V	N9
J2.84	LVDS RX bit 6 or CMOS bit 29	HSMB_RX_D_P6	LVDS or 2.5-V	M6
J2.85	LVDS TX bit 6n or CMOS bit 30	HSMB_TX_D_N6	LVDS or 2.5-V	P8
J2.86	LVDS RX bit 6n or CMOS bit 31	HSMB_RX_D_N6	LVDS or 2.5-V	L5
J2.89	LVDS TX bit 7 or CMOS bit 32	HSMB_TX_D_P7	LVDS or 2.5-V	N11
J2.90	LVDS RX bit 7 or CMOS bit 33	HSMB_RX_D_P7	LVDS or 2.5-V	K6

Table 2–38. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J2.91	LVDS TX bit 7n or CMOS bit 34	HSMB_TX_D_N7	LVDS or 2.5-V	N10
J2.92	LVDS RX bit 7n or CMOS bit 35	HSMB_RX_D_N7	LVDS or 2.5-V	K5
J2.95	LVDS or CMOS clock out 1 or CMOS bit 36	HSMB_CLK_OUT_P1	LVDS or 2.5-V	K8
J2.96	LVDS or CMOS clock in 1 or CMOS bit 37	HSMB_CLK_IN_P1	LVDS or 2.5-V	AB6
J2.97	LVDS or CMOS clock out 1 or CMOS bit 38	HSMB_CLK_OUT_N1	LVDS or 2.5-V	J8
J2.98	LVDS or CMOS clock in 1 or CMOS bit 39	HSMB_CLK_IN_N1	LVDS or 2.5-V	AA5
J2.101	LVDS TX bit 8 or CMOS bit 40	HSMB_TX_D_P8	LVDS or 2.5-V	M8
J2.102	LVDS RX bit 8 or CMOS bit 41	HSMB_RX_D_P8	LVDS or 2.5-V	J6
J2.103	LVDS TX bit 8n or CMOS bit 42	HSMB_TX_D_N8	LVDS or 2.5-V	M7
J2.104	LVDS RX bit 8n or CMOS bit 43	HSMB_RX_D_N8	LVDS or 2.5-V	J5
J2.107	LVDS TX bit 9 or CMOS bit 44	HSMB_TX_D_P9	LVDS or 2.5-V	L8
J2.108	LVDS RX bit 9 or CMOS bit 45	HSMB_RX_D_P9	LVDS or 2.5-V	G8
J2.109	LVDS TX bit 9n or CMOS bit 46	HSMB_TX_D_N9	LVDS or 2.5-V	L7
J2.110	LVDS RX bit 9n or CMOS bit 47	HSMB_RX_D_N9	LVDS or 2.5-V	F8
J2.113	LVDS TX bit 10 or CMOS bit 48	HSMB_TX_D_P10	LVDS or 2.5-V	K7
J2.114	LVDS RX bit 10 or CMOS bit 49	HSMB_RX_D_P10	LVDS or 2.5-V	G6
J2.115	LVDS TX bit 10n or CMOS bit 50	HSMB_TX_D_N10	LVDS or 2.5-V	J7
J2.116	LVDS RX bit 10n or CMOS bit 51	HSMB_RX_D_N10	LVDS or 2.5-V	F6
J2.119	LVDS TX bit 11 or CMOS bit 52	HSMB_TX_D_P11	LVDS or 2.5-V	K9
J2.120	LVDS RX bit 11 or CMOS bit 53	HSMB_RX_D_P11	LVDS or 2.5-V	G5
J2.121	LVDS TX bit 11n or CMOS bit 54	HSMB_TX_D_N11	LVDS or 2.5-V	J9
J2.122	LVDS RX bit 11n or CMOS bit 55	HSMB_RX_D_N11	LVDS or 2.5-V	F5
J2.125	LVDS TX bit 12 or CMOS bit 56	HSMB_TX_D_P12	LVDS or 2.5-V	H7
J2.126	LVDS RX bit 12 or CMOS bit 57	HSMB_RX_D_P12	LVDS or 2.5-V	F7
J2.127	LVDS TX bit 12n or CMOS bit 58	HSMB_TX_D_N12	LVDS or 2.5-V	G7
J2.128	LVDS RX bit 12n or CMOS bit 59	HSMB_RX_D_N12	LVDS or 2.5-V	E7
J2.131	LVDS TX bit 13 or CMOS bit 60	HSMB_TX_D_P13	LVDS or 2.5-V	M10
J2.132	LVDS RX bit 13 or CMOS bit 61	HSMB_RX_D_P13	LVDS or 2.5-V	G9
J2.133	LVDS TX bit 13n or CMOS bit 62	HSMB_TX_D_N13	LVDS or 2.5-V	L10
J2.134	LVDS RX bit 13n or CMOS bit 63	HSMB_RX_D_N13	LVDS or 2.5-V	F9
J2.137	LVDS TX bit 14 or CMOS bit 64	HSMB_TX_D_P14	LVDS or 2.5-V	R12
J2.138	LVDS RX bit 14 or CMOS bit 65	HSMB_RX_D_P14	LVDS or 2.5-V	D7
J2.139	LVDS TX bit 14n or CMOS bit 66	HSMB_TX_D_N14	LVDS or 2.5-V	R11
J2.140	LVDS RX bit 14n or CMOS bit 67	HSMB_RX_D_N14	LVDS or 2.5-V	C7
J2.143	LVDS TX bit 15 or CMOS bit 68	HSMB_TX_D_P15	LVDS or 2.5-V	T13
J2.144	LVDS RX bit 15 or CMOS bit 69	HSMB_RX_D_P15	LVDS or 2.5-V	D8
J2.145	LVDS TX bit 15n or CMOS bit 70	HSMB_TX_D_N15	LVDS or 2.5-V	T12
J2.146	LVDS RX bit 15n or CMOS bit 71	HSMB_RX_D_N15	LVDS or 2.5-V	C8

Table 2–38. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
J2.149	LVDS TX bit 16 or CMOS bit 72	HSMB_TX_D_P16	LVDS or 2.5-V	R13
J2.150	LVDS RX bit 16 or CMOS bit 73	HSMB_RX_D_P16	LVDS or 2.5-V	F10
J2.151	LVDS TX bit 16n or CMOS bit 74	HSMB_TX_D_N16	LVDS or 2.5-V	P13
J2.152	LVDS RX bit 16n or CMOS bit 75	HSMB_RX_D_N16	LVDS or 2.5-V	E10
J2.155	LVDS or CMOS clock out 2 or CMOS bit 76	HSMB_CLK_OUT_P2	LVDS or 2.5-V	K10
J2.156	LVDS or CMOS clock in 2 or CMOS bit 77	HSMB_CLK_IN_P2	LVDS or 2.5-V	W6
J2.157	LVDS or CMOS clock out 2 or CMOS bit 78	HSMB_CLK_OUT_N2	LVDS or 2.5-V	J10
J2.158	LVDS or CMOS clock in 2 or CMOS bit 79	HSMB_CLK_IN_N2	LVDS or 2.5-V	W5
J2.160	HSMC Port B presence detect	HSMB_PRSNTn	2.5-V	D9
D15	User LED to show RX data activity on HSMC Port B	HSMB_RX_LED	2.5-V	AT10
D14	User LED to show TX data activity on HSMC Port B	HSMB_TX_LED	2.5-V	AH33

Table 2–39 lists the HSMC connector component reference and manufacturing information.

Table 2–39. HSMC Connector Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
J1 and J2	HSMC, custom version of QSH-DP family high-speed socket.	Samtec	ASP-122953-01	www.samtec.com

HDMI Video Output

The Stratix IV GX FPGA development board includes a single HDMI video output port based on the Analog Devices AD9889B HDMI transmitter device.

With the capability of up to 80 MHz operation, this device supports all video resolutions from 480i to 1080i and UXGA at 60 Hz. This device also features a programmable two-way color space converter which supports RGB, YCbCr, and DDR, as well as ITU656-based embedded syncs and an automatic input video format timing detection (CEA-861B) circuit.

On the digital audio aspect, this device supports standard S/PDIF for stereo LPCM or compressed audio of up to 192 kHz. This device also supports 8-channel, uncompressed, LPCM I2S audio of up to 192 kHz. No audio master clock is needed for supporting S/PDIF and I2S.

This device supports an on-chip microcontroller (MCU) with I^{2}C® master to perform HDCP operations and EDID reading operations although the board does not have an HDCP EEPROM installed by default. The on-chip MPU, accessible from the FPGA through the serial port, reports HDMI events through interrupts and registers.

Figure 2–12 shows a block diagram of the AD9889B HDMI transmitter device.

Figure 2–12. AD9889B HDMI Transmitter Device Block Diagram

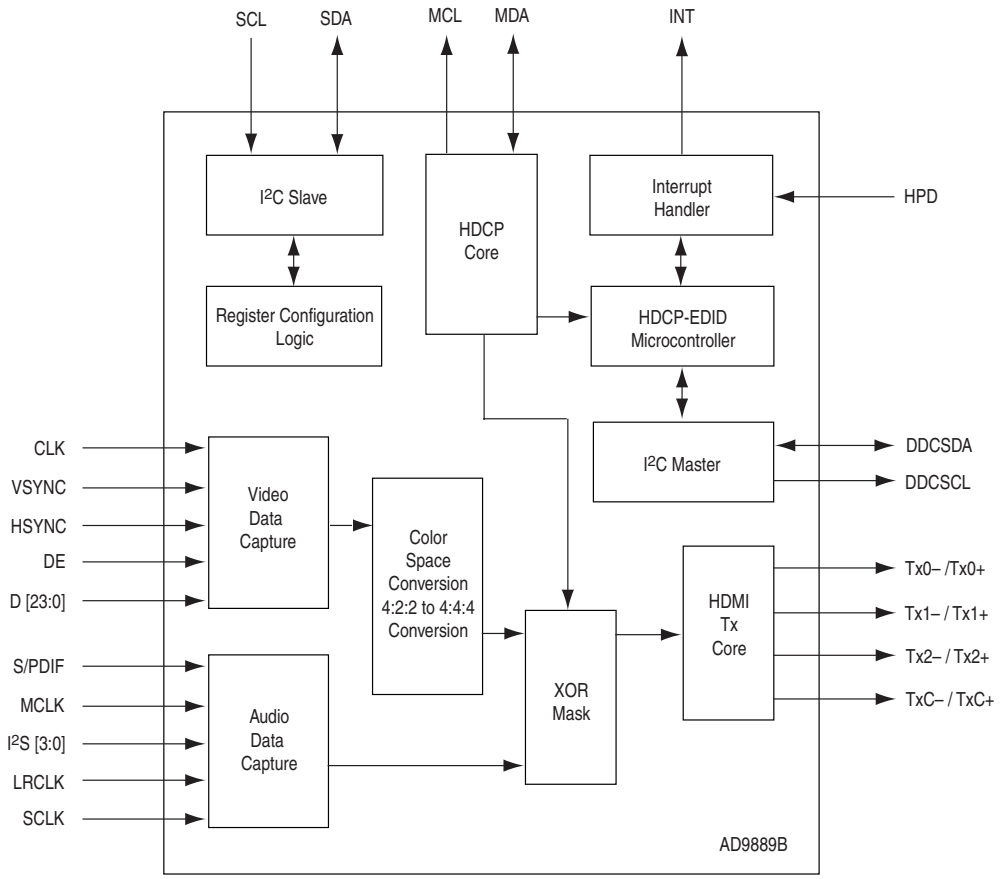


Table 2–40 lists the HDMI video output interface pin assignments, signal names, and functions.

Table 2–40. HDMI Video Output Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U25.B1	Video data bus	HDMI_D0	1.8-V	AW34
U25.A1	Video data bus	HDMI_D1	1.8-V	AL25
U25.B2	Video data bus	HDMI_D2	1.8-V	AK25
U25.A2	Video data bus	HDMI_D3	1.8-V	AP26
U25.B3	Video data bus	HDMI_D4	1.8-V	AH26
U25.A3	Video data bus	HDMI_D5	1.8-V	AM26
U25.B4	Video data bus	HDMI_D6	1.8-V	AK26
U25.A4	Video data bus	HDMI_D7	1.8-V	AN26
U25.B5	Video data bus	HDMI_D8	1.8-V	AP27
U25.A5	Video data bus	HDMI_D9	1.8-V	AN27

Table 2–40. HDMI Video Output Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U25.B6	Video data bus	HDMI_D10	1.8-V	AV28
U25.A6	Video data bus	HDMI_D11	1.8-V	AW29
U25.B7	Video data bus	HDMI_D12	1.8-V	AW27
U25.A7	Video data bus	HDMI_D13	1.8-V	AW28
U25.B8	Video data bus	HDMI_D14	1.8-V	AV29
U25.A8	Video data bus	HDMI_D15	1.8-V	AW30
U25.B9	Video data bus	HDMI_D16	1.8-V	AW31
U25.A9	Video data bus	HDMI_D17	1.8-V	AV31
U25.B10	Video data bus	HDMI_D18	1.8-V	AV32
U25.A10	Video data bus	HDMI_D19	1.8-V	AW32
U25.C9	Video data bus	HDMI_D20	1.8-V	AW33
U25.C10	Video data bus	HDMI_D21	1.8-V	AJ25
U25.D9	Video data bus	HDMI_D22	1.8-V	AL27
U25.D10	Video data bus	HDMI_D23	1.8-V	AJ26
U25.D1	Video data bus clock	HDMI_CLK	1.8-V	AD25
U25.C2	Video data bus DE	HDMI_DE	1.8-V	AK27
U25.C1	Video data bus HSYNC	HDMI_HSYNC	1.8-V	AE24
U25.D2	Video data bus VSYNC	HDMI_VSYNC	1.8-V	AE25
U25.E2	Audio SPDIF data	HDMI_SPDIF	1.8-V	AR28
U25.E1	Audio SPDIF clock	HDMI_MCLK	1.8-V	AP28
U25.F2	Audio I²S bus	HDMI_I2S0	1.8-V	AT29
U25.F1	Audio I²S bus	HDMI_I2S1	1.8-V	AU29
U25.G2	Audio I²S bus	HDMI_I2S2	1.8-V	AU28
U25.G1	Audio I²S bus	HDMI_I2S3	1.8-V	AT28
U25.H2	Audio I²S bus clock	HDMI_SCLK	1.8-V	AH24
U25.H1	Audio LR clock	HDMI_LRCLK	1.8-V	AG24
U25.F9	Management bus clock	HDMI_SDA	1.8-V	AU27
U25.F10	Management bus data	HDMI_SCL	1.8-V	AT27
U25.H10	Management bus interrupt	HDMI_INTn	1.8-V	AV23

Table 2–41 lists the HDMI video output component reference and manufacturing information.

Table 2–41. HDMI Video Output Connector Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U25	HDMI transmitter	Analog Devices	AD9889BBBCZ-80	www.analog.com

SDI Video Input/Output

The SDI video port consists of a LMH0302SQ cable driver and a LMH0344 receiver cable equalizer. The PHY devices from National Semiconductor interface to single-ended 75-Ω SMB connectors and extends out through the PCI Express bracket for easy use while installed in a host PC.

The LMH0302SQ driver supports operation at 270 Mbit standard definition (SD), 1.5 Gbit high definition (HD), and 3.0 Gbit dual-link HD modes. Control signals for SD and HD modes selections, as well as device enable can be set. The device can be clocked by the 148.5 MHz voltage-controlled crystal oscillator (VCXO) and matched to incoming signals within 50 ppm using the UP and DN voltage control lines to the VCXO.

Table 2–42 lists the supported output standards for the SD and HD input.

Table 2–42. Supported Output Standards for SD and HD Input

SD_HD Input	Supported Output Standards	Rise TIme
0	SMPTE 424M, SMPTE 292M	Faster
1	SMPTE 259M	Slower

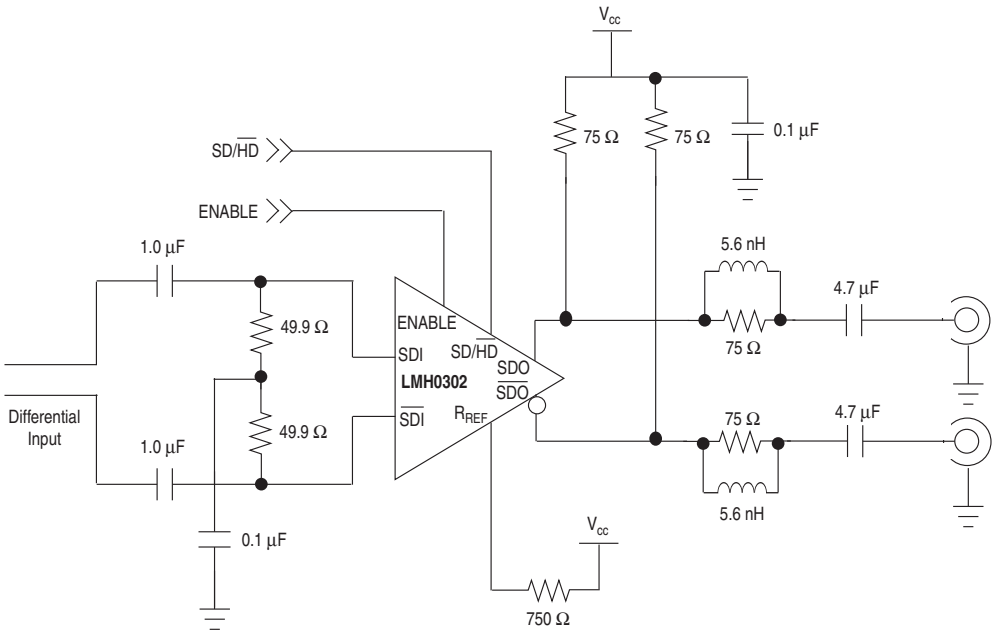
Table 2–43 lists the SDI video output interface pin assignments. The signal names and directions are relative to the Stratix IV GX FPGA.

Table 2–43. SDI Video Output Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U4.1	SDI video output P	SDI_TX_P	1.4-V PCML	K4
U4.2	SDI video output N	SDI_TX_N		K3
U4.6	Device enable	SDI_TX_EN	2.5-V	N6
U4.10	High definition select	SDI_TX_SD_HDn		V29

Figure 2–13 shows the SDI cable driver.

Figure 2–13. SDI Cable Driver



The LMH0344 cable equalizer supports operation at 270 Mbit SD, 1.5 Gbit HD, and 3.0 Gbit dual-link HD modes. Control signals are allowed for bypassing or disabling the device, as well as a carrier detect or auto-mute signal interface.

Table 2–44 lists the cable equalizer lengths.

Table 2–44. SDI Cable Equalizer Lengths

Data Rate (Mbps)	Cable Type	Maximum Cable Length (m)
270	Belden 1694A	400
1485		140
2970		120

Table 2–45 lists the SDI video input interface pin assignments. The signal names and directions are relative to the Stratix IV GX FPGA.

Table 2–45. SDI Video Input Interface Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

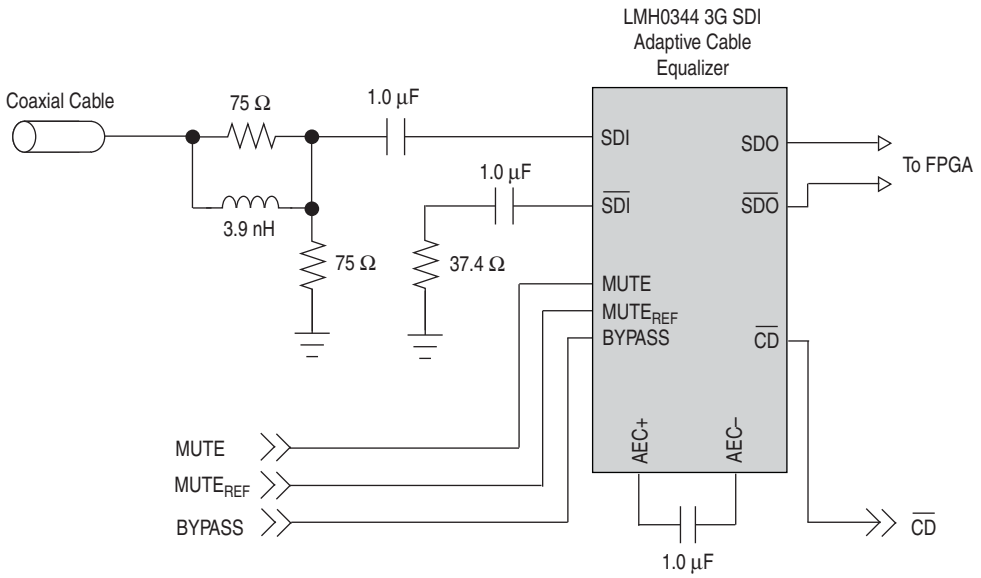
Board Reference	Description	Schematic Signal Name	I/O Standard	MAX II CPLD EPM2210 System Controller Pin Number	Stratix IV GX Device Pin Number
U2.11	SDI video input P	SDI_RX_P	1.4-V PCML	—	L2
U2.10	SDI video input N	SDI_RX_N	1.4-V PCML	—	L1

Table 2–45. SDI Video Input Interface Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX II CPLD EPM2210 System Controller Pin Number	Stratix IV GX Device Pin Number
U2.7	Bypass enable	SDI_RX_BYPASS	2.5-V	T4	—
U2.14	Device enable	SDI_RX_EN	2.5-V	M6	— (Automatically driven by carrier detect)

Figure 2–14 shows the SDI cable equalizer.

Figure 2–14. SDI Cable Equalizer



Memory

This section describes the board's memory interface support, signal names, types, and connectivity relative to the Stratix IV GX device. The board has the following memory interfaces:

- DDR3 bottom port
- DDR3 top port
- QDRII+ top port 0
- QDRII+ top port 1
- SSRAM
- Flash

For more information about the memory interfaces, refer to the External Memory Interface Handbook.

DDR3 Bottom Port

The DDR3 bottom port consists of four DDR3 devices, providing a single 512-Mbyte interface with a 64-bit data bus. The board supports addressing for up to 4 times the memory if larger devices become available.

This memory interface is designed to run between 300 MHz, the minimum frequency for DDR3, and 533 MHz for a maximum theoretical bandwidth of over 68.2 Gbps. The internal bus in the FPGA is typically 2 or 4 times the width at full-rate or half-rate respectively. For example, a 533 MHz 64-bit interface will become a 267 MHz 256-bit bus.

Table 2–46 lists the DDR3 DIMM pin assignments, signal names, and functions. The signal names and types are relative to the Stratix IV device in terms of I/O setting and direction.

Table 2–46. DDR3 Bottom Port Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U5, U12, U18, U24 pin T7	Address bus	DDR3BOT_A14	1.5-V SSTL Class I	AJ14
U5, U12, U18, U24 pin T3	Address bus	DDR3BOT_A13	1.5-V SSTL Class I	AN15
U5, U12, U18, U24 pin N7	Address bus	DDR3BOT_A12	1.5-V SSTL Class I	AE14
U5, U12, U18, U24 pin R7	Address bus	DDR3BOT_A11	1.5-V SSTL Class I	AJ13
U5, U12, U18, U24 pin L7	Address bus	DDR3BOT_A10	1.5-V SSTL Class I	AE16
U5, U12, U18, U24 pin R3	Address bus	DDR3BOT_A9	1.5-V SSTL Class I	AK14
U5, U12, U18, U24 pin T8	Address bus	DDR3BOT_A8	1.5-V SSTL Class I	AH13
U5, U12, U18, U24 pin R2	Address bus	DDR3BOT_A7	1.5-V SSTL Class I	AP15
U5, U12, U18, U24 pin R8	Address bus	DDR3BOT_A6	1.5-V SSTL Class I	AG14
U5, U12, U18, U24 pin P2	Address bus	DDR3BOT_A5	1.5-V SSTL Class I	AL15
U5, U12, U18, U24 pin P8	Address bus	DDR3BOT_A4	1.5-V SSTL Class I	AF16
U5, U12, U18, U24 pin N2	Address bus	DDR3BOT_A3	1.5-V SSTL Class I	AT14
U5, U12, U18, U24 pin P3	Address bus	DDR3BOT_A2	1.5-V SSTL Class I	AH14
U5, U12, U18, U24 pin P7	Address bus	DDR3BOT_A1	1.5-V SSTL Class I	AG15
U5, U12, U18, U24 pin N3	Address bus	DDR3BOT_A0	1.5-V SSTL Class I	AK13
U5, U12, U18, U24 pin M3	Bank address bus	DDR3BOT_BA2	1.5-V SSTL Class I	AE15
U5, U12, U18, U24 pin M3	Bank address bus	DDR3BOT_BA1	1.5-V SSTL Class I	AD15
U5, U12, U18, U24 pin M3	Bank address bus	DDR3BOT_BA0	1.5-V SSTL Class I	AF14
U5, U12, U18, U24 pin J3	Row address select	DDR3BOT_RASn	1.5-V SSTL Class I	AW21
U5, U12, U18, U24 pin T2	Reset	DDR3BOT_RSTn	1.5-V SSTL Class I	AP20
U5, U12, U18, U24 pin K3	Column address select	DDR3BOT_CASn	1.5-V SSTL Class I	AV19
U5, U12, U18, U24 pin L2	Chip select	DDR3BOT_CSn	1.5-V SSTL Class I	AN20
U5, U12, U18, U24 pin L3	Write enable	DDR3BOT_WEn	1.5-V SSTL Class I	AW20
U5, U12, U18, U24 pin K1	Termination enable	DDR3BOT_ODT	1.5-V SSTL Class I	AU20
U5, U12, U18, U24 pin K9	Clock enable	DDR3BOT_CKE	1.5-V SSTL Class I	AW19
U5, U12, U18, U24 pin J7	Clock P	DDR3BOT_CK_P	1.5-V SSTL Class I	AE20

Table 2–46. DDR3 Bottom Port Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U5, U12, U18, U24 pin K7	Clock N	DDR3BOT_CK_N	1.5-V SSTL Class I	AF20
U5.E3	Data bus byte lane 0	DDR3BOT_DQ0	1.5-V SSTL Class I	AM14
U5.F7	Data bus byte lane 0	DDR3BOT_DQ1	1.5-V SSTL Class I	AM13
U5.F2	Data bus byte lane 0	DDR3BOT_DQ2	1.5-V SSTL Class I	AN14
U5.F8	Data bus byte lane 0	DDR3BOT_DQ3	1.5-V SSTL Class I	AL14
U5.H3	Data bus byte lane 0	DDR3BOT_DQ4	1.5-V SSTL Class I	AR14
U5.H8	Data bus byte lane 0	DDR3BOT_DQ5	1.5-V SSTL Class I	AN13
U5.G2	Data bus byte lane 0	DDR3BOT_DQ6	1.5-V SSTL Class I	AP14
U5.H7	Data bus byte lane 0	DDR3BOT_DQ7	1.5-V SSTL Class I	AP13
U5.E7	Write mask byte lane 0	DDR3BOT_DM0	1.5-V SSTL Class I	AL13
U5.F3	Data strobe P byte lane 0	DDR3BOT_DQS_P0	1.5-V SSTL Class I	AR13
U5.G3	Data strobe N byte lane 0	DDR3BOT_DQS_N0	1.5-V SSTL Class I	AT13
U5.D7	Data bus byte lane 1	DDR3BOT_DQ8	1.5-V SSTL Class I	AT12
U5.C3	Data bus byte lane 1	DDR3BOT_DQ9	1.5-V SSTL Class I	AW14
U5.C8	Data bus byte lane 1	DDR3BOT_DQ10	1.5-V SSTL Class I	AU12
U5.C2	Data bus byte lane 1	DDR3BOT_DQ11	1.5-V SSTL Class I	AV14
U5.A7	Data bus byte lane 1	DDR3BOT_DQ12	1.5-V SSTL Class I	AW11
U5.A2	Data bus byte lane 1	DDR3BOT_DQ13	1.5-V SSTL Class I	AU14
U5.B8	Data bus byte lane 1	DDR3BOT_DQ14	1.5-V SSTL Class I	AV11
U5.A3	Data bus byte lane 1	DDR3BOT_DQ15	1.5-V SSTL Class I	AW12
U5.D3	Write mask byte lane 1	DDR3BOT_DM1	1.5-V SSTL Class I	AU11
U5.C7	Data strobe P byte lane 1	DDR3BOT_DQS_P1	1.5-V SSTL Class I	AV13
U5.B7	Data strobe N byte lane 1	DDR3BOT_DQS_N1	1.5-V SSTL Class I	AW13
U12.E3	Data bus byte lane 2	DDR3BOT_DQ16	1.5-V SSTL Class I	AT16
U12.F7	Data bus byte lane 2	DDR3BOT_DQ17	1.5-V SSTL Class I	AW16
U12.F2	Data bus byte lane 2	DDR3BOT_DQ18	1.5-V SSTL Class I	AN16
U12.F8	Data bus byte lane 2	DDR3BOT_DQ19	1.5-V SSTL Class I	AV16
U12.H3	Data bus byte lane 2	DDR3BOT_DQ20	1.5-V SSTL Class I	AP17
U12.H8	Data bus byte lane 2	DDR3BOT_DQ21	1.5-V SSTL Class I	AT15
U12.G2	Data bus byte lane 2	DDR3BOT_DQ22	1.5-V SSTL Class I	AR17
U12.H7	Data bus byte lane 2	DDR3BOT_DQ23	1.5-V SSTL Class I	AU15
U12.E7	Write mask byte lane 2	DDR3BOT_DM2	1.5-V SSTL Class I	AU16
U12.F3	Data strobe P byte lane 2	DDR3BOT_DQS_P2	1.5-V SSTL Class I	AP16
U12.G3	Data strobe N byte lane 2	DDR3BOT_DQS_N2	1.5-V SSTL Class I	AR16
U12.D7	Data bus byte lane 3	DDR3BOT_DQ24	1.5-V SSTL Class I	AJ16
U12.C3	Data bus byte lane 3	DDR3BOT_DQ25	1.5-V SSTL Class I	AM17
U12.C8	Data bus byte lane 3	DDR3BOT_DQ26	1.5-V SSTL Class I	AH16
U12.C2	Data bus byte lane 3	DDR3BOT_DQ27	1.5-V SSTL Class I	AL17

Table 2–46. DDR3 Bottom Port Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U12.A7	Data bus byte lane 3	DDR3BOT_DQ28	1.5-V SSTL Class I	AG16
U12.A2	Data bus byte lane 3	DDR3BOT_DQ29	1.5-V SSTL Class I	AH17
U12.B8	Data bus byte lane 3	DDR3BOT_DQ30	1.5-V SSTL Class I	AG17
U12.A3	Data bus byte lane 3	DDR3BOT_DQ31	1.5-V SSTL Class I	AK17
U12.D3	Write mask byte lane 3	DDR3BOT_DM3	1.5-V SSTL Class I	AF17
U12.C7	Data strobe P byte lane 3	DDR3BOT_DQS_P3	1.5-V SSTL Class I	AK16
U12.B7	Data strobe N byte lane 3	DDR3BOT_DQS_N3	1.5-V SSTL Class I	AL16
U18.E3	Data bus byte lane 4	DDR3BOT_DQ32	1.5-V SSTL Class I	AU23
U18.F7	Data bus byte lane 4	DDR3BOT_DQ33	1.5-V SSTL Class I	AN23
U18.F2	Data bus byte lane 4	DDR3BOT_DQ34	1.5-V SSTL Class I	AT23
U18.F8	Data bus byte lane 4	DDR3BOT_DQ35	1.5-V SSTL Class I	AM23
U18.H3	Data bus byte lane 4	DDR3BOT_DQ36	1.5-V SSTL Class I	AP23
U18.H8	Data bus byte lane 4	DDR3BOT_DQ37	1.5-V SSTL Class I	AL22
U18.G2	Data bus byte lane 4	DDR3BOT_DQ38	1.5-V SSTL Class I	AR23
U18.H7	Data bus byte lane 4	DDR3BOT_DQ39	1.5-V SSTL Class I	AN22
U18.E7	Write mask byte lane 4	DDR3BOT_DM4	1.5-V SSTL Class I	AM22
U18.F3	Data strobe P byte lane 4	DDR3BOT_DQS_P4	1.5-V SSTL Class I	AT24
U18.G3	Data strobe N byte lane 4	DDR3BOT_DQS_N4	1.5-V SSTL Class I	AU24
U18.D7	Data bus byte lane 5	DDR3BOT_DQ40	1.5-V SSTL Class I	AR19
U18.C3	Data bus byte lane 5	DDR3BOT_DQ41	1.5-V SSTL Class I	AP19
U18.C8	Data bus byte lane 5	DDR3BOT_DQ42	1.5-V SSTL Class I	AP18
U18.C2	Data bus byte lane 5	DDR3BOT_DQ43	1.5-V SSTL Class I	AN19
U18.A7	Data bus byte lane 5	DDR3BOT_DQ44	1.5-V SSTL Class I	AT18
U18.A2	Data bus byte lane 5	DDR3BOT_DQ45	1.5-V SSTL Class I	AU18
U18.B8	Data bus byte lane 5	DDR3BOT_DQ46	1.5-V SSTL Class I	AW18
U18.A3	Data bus byte lane 5	DDR3BOT_DQ47	1.5-V SSTL Class I	AT17
U18.D3	Write mask byte lane 5	DDR3BOT_DM5	1.5-V SSTL Class I	AN18
U18.C7	Data strobe P byte lane 5	DDR3BOT_DQS_P5	1.5-V SSTL Class I	AU17
U18.B7	Data strobe N byte lane 5	DDR3BOT_DQS_N5	1.5-V SSTL Class I	AV17
U24.E3	Data bus byte lane 6	DDR3BOT_DQ48	1.5-V SSTL Class I	AV26
U24.F7	Data bus byte lane 6	DDR3BOT_DQ49	1.5-V SSTL Class I	AU25
U24.F2	Data bus byte lane 6	DDR3BOT_DQ50	1.5-V SSTL Class I	AT25
U24.F8	Data bus byte lane 6	DDR3BOT_DQ51	1.5-V SSTL Class I	AN25
U24.H3	Data bus byte lane 6	DDR3BOT_DQ52	1.5-V SSTL Class I	AR25
U24.H8	Data bus byte lane 6	DDR3BOT_DQ53	1.5-V SSTL Class I	AP24
U24.G2	Data bus byte lane 6	DDR3BOT_DQ54	1.5-V SSTL Class I	AP25
U24.H7	Data bus byte lane 6	DDR3BOT_DQ55	1.5-V SSTL Class I	AW26
U24.E7	Write mask byte lane 6	DDR3BOT_DM6	1.5-V SSTL Class I	AN24

Table 2–46. DDR3 Bottom Port Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U24.F3	Data strobe P byte lane 6	DDR3BOT_DQS_P6	1.5-V SSTL Class I	AT26
U24.G3	Data strobe N byte lane 6	DDR3BOT_DQS_N6	1.5-V SSTL Class I	AU26
U24.D7	Data bus byte lane 7	DDR3BOT_DQ56	1.5-V SSTL Class I	AJ23
U24.C3	Data bus byte lane 7	DDR3BOT_DQ57	1.5-V SSTL Class I	AK24
U24.C8	Data bus byte lane 7	DDR3BOT_DQ58	1.5-V SSTL Class I	AF23
U24.C2	Data bus byte lane 7	DDR3BOT_DQ59	1.5-V SSTL Class I	AH23
U24.A7	Data bus byte lane 7	DDR3BOT_DQ60	1.5-V SSTL Class I	AG22
U24.A2	Data bus byte lane 7	DDR3BOT_DQ61	1.5-V SSTL Class I	AJ22
U24.B8	Data bus byte lane 7	DDR3BOT_DQ62	1.5-V SSTL Class I	AH22
U24.A3	Data bus byte lane 7	DDR3BOT_DQ63	1.5-V SSTL Class I	AE22
U24.D3	Write mask byte lane 7	DDR3BOT_DM7	1.5-V SSTL Class I	AF22
U24.C7	Data strobe P byte lane 7	DDR3BOT_DQS_P7	1.5-V SSTL Class I	AK23
U24.B7	Data strobe N byte lane 7	DDR3BOT_DQS_N7	1.5-V SSTL Class I	AL23

Table 2–47 lists the DDR3 component reference and manufacturing information.

Table 2–47. DDR3 Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U5, U12, U18, U24	8 M × 16-bit × 8 banks, 667M, CL9	Micron	MT41J64M16LA-15E	www.micron.com

DDR3 Top Port

The DDR3 top port consists of a single DDR3 devices, providing 128 Mbyte with a 16-bit data bus. The board supports addressing for up to 4 times the memory if larger devices become available.

This memory interface is designed to run between 300 MHz, the minimum frequency for DDR3, and 533 MHz for a maximum theoretical bandwidth of over 68.2 Gbps. The internal bus in the FPGA is typically 2 or 4 times the width at full rate or half rate respectively. For example, a 533 MHz 64-bit interface will become a 267 MHz 256-bit bus.

Table 2–48 lists the DDR3 top port pin assignments, signal names, and its functions. The signal names and types are relative to the Stratix IV device in terms of I/O setting and direction.

Table 2–48. DDR3 Top Port Pin Assignments, Signal Names and Functions (Part 1 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U14.T7	Address bus	DDR3TOP_A14	1.5-V SSTL Class I	B20
U14.T3	Address bus	DDR3TOP_A13	1.5-V SSTL Class I	M22
U14.N7	Address bus	DDR3TOP_A12	1.5-V SSTL Class I	A23

Table 2–48. DDR3 Top Port Pin Assignments, Signal Names and Functions (Part 2 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U14.R7	Address bus	DDR3TOP_A11	1.5-V SSTL Class I	A19
U14.L7	Address bus	DDR3TOP_A10	1.5-V SSTL Class I	B23
U14.R3	Address bus	DDR3TOP_A9	1.5-V SSTL Class I	M21
U14.T8	Address bus	DDR3TOP_A8	1.5-V SSTL Class I	F21
U14.R2	Address bus	DDR3TOP_A7	1.5-V SSTL Class I	M20
U14.R8	Address bus	DDR3TOP_A6	1.5-V SSTL Class I	G21
U14.P2	Address bus	DDR3TOP_A5	1.5-V SSTL Class I	P19
U14.P8	Address bus	DDR3TOP_A4	1.5-V SSTL Class I	D21
U14.N2	Address bus	DDR3TOP_A3	1.5-V SSTL Class I	R20
U14.P3	Address bus	DDR3TOP_A2	1.5-V SSTL Class I	N19
U14.P7	Address bus	DDR3TOP_A1	1.5-V SSTL Class I	C22
U14.N3	Address bus	DDR3TOP_A0	1.5-V SSTL Class I	D19
U14.M3	Bank address bus	DDR3TOP_BA2	1.5-V SSTL Class I	A14
U14.N8	Bank address bus	DDR3TOP_BA1	1.5-V SSTL Class I	E23
U14.M2	Bank address bus	DDR3TOP_BA0	1.5-V SSTL Class I	B14
U14.J3	Row address select	DDR3TOP_RASn	1.5-V SSTL Class I	A24
U14.T2	Reset	DDR3TOP_RSTn	1.5-V SSTL Class I	L20
U14.K3	Column address select	DDR3TOP_CASn	1.5-V SSTL Class I	B19
U14.L2	Chip select	DDR3TOP_CSn	1.5-V SSTL Class I	D15
U14.L3	Write enable	DDR3TOP_WEn	1.5-V SSTL Class I	C19
U14.K1	Termination enable	DDR3TOP_ODT	1.5-V SSTL Class I	K15
U14.K9	Clock enable	DDR3TOP_CKE	1.5-V SSTL Class I	A25
U14.J7	Clock P	DDR3TOP_CK_P	1.5-V SSTL Class I	D24
U14.K7	Clock N	DDR3TOP_CK_N	1.5-V SSTL Class I	C24
U14.E3	Data bus byte lane 0	DDR3TOP_DQ0	1.5-V SSTL Class I	A10
U14.F7	Data bus byte lane 0	DDR3TOP_DQ1	1.5-V SSTL Class I	D11
U14.F2	Data bus byte lane 0	DDR3TOP_DQ2	1.5-V SSTL Class I	B10
U14.F8	Data bus byte lane 0	DDR3TOP_DQ3	1.5-V SSTL Class I	C12
U14.H3	Data bus byte lane 0	DDR3TOP_DQ4	1.5-V SSTL Class I	C11
U14.H8	Data bus byte lane 0	DDR3TOP_DQ5	1.5-V SSTL Class I	C13
U14.G2	Data bus byte lane 0	DDR3TOP_DQ6	1.5-V SSTL Class I	A11
U14.H7	Data bus byte lane 0	DDR3TOP_DQ7	1.5-V SSTL Class I	B13
U14.E7	Write mask byte lane 0	DDR3TOP_DM0	1.5-V SSTL Class I	B11
U14.F3	Data strobe P byte lane 0	DDR3TOP_DQS_P0	1.5-V SSTL Class I	D14
U14.G3	Data strobe N byte lane 0	DDR3TOP_DQS_N0	1.5-V SSTL Class I	C14
U14.D7	Data bus byte lane 1	DDR3TOP_DQ8	1.5-V SSTL Class I	K22
U14.C3	Data bus byte lane 1	DDR3TOP_DQ9	1.5-V SSTL Class I	D22
U14.C8	Data bus byte lane 1	DDR3TOP_DQ10	1.5-V SSTL Class I	J22

Table 2–48. DDR3 Top Port Pin Assignments, Signal Names and Functions (Part 3 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U14.C2	Data bus byte lane 1	DDR3TOP_DQ11	1.5-V SSTL Class I	E22
U14.A7	Data bus byte lane 1	DDR3TOP_DQ12	1.5-V SSTL Class I	G22
U14.A2	Data bus byte lane 1	DDR3TOP_DQ13	1.5-V SSTL Class I	F23
U14.B8	Data bus byte lane 1	DDR3TOP_DQ14	1.5-V SSTL Class I	H22
U14.A3	Data bus byte lane 1	DDR3TOP_DQ15	1.5-V SSTL Class I	D23
U14.D3	Write mask byte lane 1	DDR3TOP_DM1	1.5-V SSTL Class I	G23
U14.C7	Data strobe P byte lane 1	DDR3TOP_DQS_P1	1.5-V SSTL Class I	J23
U14.B7	Data strobe N byte lane 1	DDR3TOP_DQS_N1	1.5-V SSTL Class I	H23

Table 2–49 lists the DDR3 component reference and manufacturing information.

Table 2–49. DDR3 Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U14	8 M × 16-bit × 8 banks, 667M, CL9	Micron	MT41J64M16LA-15E	www.micron.com

QDRII+ Top Port 0

The QDRII+ top port 0 consists of a single QDRII+ burst-of-4 SRAM, providing 4 Mbyte with an 18-bit read data bus and an 18-bit write data bus.

This memory interface is designed to run between 120 MHz, the minimum frequency for this device, and 400 MHz for a maximum theoretical bandwidth of over 14.4 Gbps for reading and 14.4 Gbps for writing. The internal bus in the FPGA is typically 2 or 4 times the width at full rate or half rate respectively. For example, a 400 MHz 18-bit interface becomes a 200 MHz 72 bit bus.

Table 2–50 lists the QDRII+ top port 0 pin assignments, signal names, and functions. The signal names and types are relative to the Stratix IV GX device in terms of I/O setting and direction.

Table 2–50. QDRII+ Top Port 0 Pin Assignments, Signal Names and Functions (Part 1 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U22.A10	Address bus	QDR2TOP0_A19	1.5-V HSTL Class I	A28
U22.A3	Address bus	QDR2TOP0_A18	1.5-V HSTL Class I	J24
U22.A9	Address bus	QDR2TOP0_A17	1.5-V HSTL Class I	C28
U22.R7	Address bus	QDR2TOP0_A16	1.5-V HSTL Class I	G28
U22.R5	Address bus	QDR2TOP0_A15	1.5-V HSTL Class I	C30
U22.R4	Address bus	QDR2TOP0_A14	1.5-V HSTL Class I	C29
U22.R3	Address bus	QDR2TOP0_A13	1.5-V HSTL Class I	B28
U22.P8	Address bus	QDR2TOP0_A12	1.5-V HSTL Class I	R24
U22.P7	Address bus	QDR2TOP0_A11	1.5-V HSTL Class I	N20

Table 2–50. QDRII+ Top Port 0 Pin Assignments, Signal Names and Functions (Part 2 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U22.P5	Address bus	QDR2TOP0_A10	1.5-V HSTL Class I	A31
U22.P4	Address bus	QDR2TOP0_A9	1.5-V HSTL Class I	A29
U22.N7	Address bus	QDR2TOP0_A8	1.5-V HSTL Class I	P20
U22.N6	Address bus	QDR2TOP0_A7	1.5-V HSTL Class I	B31
U22.N5	Address bus	QDR2TOP0_A6	1.5-V HSTL Class I	B29
U22.C7	Address bus	QDR2TOP0_A5	1.5-V HSTL Class I	D27
U22.C5	Address bus	QDR2TOP0_A4	1.5-V HSTL Class I	F26
U22.B8	Address bus	QDR2TOP0_A3	1.5-V HSTL Class I	A27
U22.B4	Address bus	QDR2TOP0_A2	1.5-V HSTL Class I	G26
U22.R8	Address bus	QDR2TOP0_A1	1.5-V HSTL Class I	P24
U22.R9	Address bus	QDR2TOP0_A0	1.5-V HSTL Class I	N21
U22.N2	Write data bus	QDR2TOP0_D17	1.5-V HSTL Class I	B25
U22.M3	Write data bus	QDR2TOP0_D16	1.5-V HSTL Class I	G24
U22.L3	Write data bus	QDR2TOP0_D15	1.5-V HSTL Class I	F24
U22.J3	Write data bus	QDR2TOP0_D14	1.5-V HSTL Class I	M24
U22.G2	Write data bus	QDR2TOP0_D13	1.5-V HSTL Class I	K23
U22.F3	Write data bus	QDR2TOP0_D12	1.5-V HSTL Class I	M23
U22.D2	Write data bus	QDR2TOP0_D11	1.5-V HSTL Class I	R22
U22.C3	Write data bus	QDR2TOP0_D10	1.5-V HSTL Class I	N22
U22.B3	Write data bus	QDR2TOP0_D9	1.5-V HSTL Class I	P22
U22.C11	Write data bus	QDR2TOP0_D8	1.5-V HSTL Class I	A26
U22.D11	Write data bus	QDR2TOP0_D7	1.5-V HSTL Class I	B26
U22.E10	Write data bus	QDR2TOP0_D6	1.5-V HSTL Class I	C25
U22.G11	Write data bus	QDR2TOP0_D5	1.5-V HSTL Class I	C26
U22.J11	Write data bus	QDR2TOP0_D4	1.5-V HSTL Class I	D25
U22.K10	Write data bus	QDR2TOP0_D3	1.5-V HSTL Class I	D26
U22.M11	Write data bus	QDR2TOP0_D2	1.5-V HSTL Class I	E25
U22.N11	Write data bus	QDR2TOP0_D1	1.5-V HSTL Class I	G25
U22.P10	Write data bus	QDR2TOP0_D0	1.5-V HSTL Class I	F25
U22.B6	Write clock P	QDR2TOP0_K_P	1.5-V HSTL Class I	P23
U22.A6	Write clock N	QDR2TOP0_K_N	1.5-V HSTL Class I	N23
U22.A4	Write port select	QDR2TOP0_WPSn	1.5-V HSTL Class I	K24
U22.B7	Write byte write select 0	QDR2TOP0_BWSn0	1.5-V HSTL Class I	L23
U22.A5	Write byte write select 1	QDR2TOP0_BWSn1	1.5-V HSTL Class I	J25
U22.R6	Termination enable	QDR2TOP0_ODT	1.5-V HSTL Class I	A22
U22.P3	Read data bus	QDR2TOP0_Q17	1.5-V HSTL Class I	M25
U22.N3	Read data bus	QDR2TOP0_Q16	1.5-V HSTL Class I	L25
U22.L2	Read data bus	QDR2TOP0_Q15	1.5-V HSTL Class I	N25

Table 2–50. QDRII+ Top Port 0 Pin Assignments, Signal Names and Functions (Part 3 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U22.K3	Read data bus	QDR2TOP0_Q14	1.5-V HSTL Class I	P25
U22.G3	Read data bus	QDR2TOP0_Q13	1.5-V HSTL Class I	G27
U22.F2	Read data bus	QDR2TOP0_Q12	1.5-V HSTL Class I	F27
U22.E3	Read data bus	QDR2TOP0_Q11	1.5-V HSTL Class I	D28
U22.D3	Read data bus	QDR2TOP0_Q10	1.5-V HSTL Class I	E28
U22.B2	Read data bus	QDR2TOP0_Q9	1.5-V HSTL Class I	D29
U22.B11	Read data bus	QDR2TOP0_Q8	1.5-V HSTL Class I	E29
U22.C10	Read data bus	QDR2TOP0_Q7	1.5-V HSTL Class I	F28
U22.E11	Read data bus	QDR2TOP0_Q6	1.5-V HSTL Class I	G29
U22.F11	Read data bus	QDR2TOP0_Q5	1.5-V HSTL Class I	J26
U22.J10	Read data bus	QDR2TOP0_Q4	1.5-V HSTL Class I	K26
U22.K11	Read data bus	QDR2TOP0_Q3	1.5-V HSTL Class I	J27
U22.L11	Read data bus	QDR2TOP0_Q2	1.5-V HSTL Class I	L26
U22.M10	Read data bus	QDR2TOP0_Q1	1.5-V HSTL Class I	K28
U22.P11	Read data bus	QDR2TOP0_Q0	1.5-V HSTL Class I	M27
U22.A11	Read clock P	QDR2TOP0_CQ_P	1.5-V HSTL Class I	H28
U22.A1	Read clock N	QDR2TOP0_CQ_N	1.5-V HSTL Class I	K27
U22.A8	Read port select	QDR2TOP0_RPSn	1.5-V HSTL Class I	C27
U22.P6	Read data valid	QDR2TOP0_QVLD	1.5-V HSTL Class I	H26
U22.H1	DLL enable	QDR2TOP0_DOFFn	1.5-V HSTL Class I	B22

Table 2–51 lists the QDRII+ top port 0 component reference and manufacturing information.

Table 2–51. QDRII+ Top Port 0 Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U22	QDRII+, 4 M × 18, 400 MHZ	Cypress	CY7C2563KV18-400BZXC	www.cypress.com
		NEC	uPD44647186AF5-E22-FQ1	www.nec.com
		Samsung	K7S3218U4C-EC40	www.samsung.com

QDRII+ Top Port 1

The QDRII+ top port 1 consists of a single QDRII+ burst-of-4 SRAM, providing 4 Mbyte with an 18-bit read data bus and an 18-bit write data bus.

This memory interface is designed to run between 120 MHz, the minimum frequency for this device, and 400 MHz for a maximum theoretical bandwidth of over 14.4 Gbps for reading and 14.4 Gbps for writing. The internal bus in the FPGA is typically 2 or 4 times the width at full rate or half rate respectively. For example, a 400 MHz 18-bit interface becomes a 200 MHz 72 bit bus.

Table 2–52 lists the QDRII+ top port 1 pin assignments, signal names, and functions. The signal names and types are relative to the Stratix IV GX device in terms of I/O setting and direction.

Table 2–52. QDRII+ Top Port 1 Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U7.A10	Address bus	QDR2TOP1_A19	1.5-V HSTL Class I	F20
U7.A3	Address bus	QDR2TOP1_A18	1.5-V HSTL Class I	B17
U7.A9	Address bus	QDR2TOP1_A17	1.5-V HSTL Class I	G20
U7.R7	Address bus	QDR2TOP1_A16	1.5-V HSTL Class I	E17
U7.R5	Address bus	QDR2TOP1_A15	1.5-V HSTL Class I	J18
U7.R4	Address bus	QDR2TOP1_A14	1.5-V HSTL Class I	M19
U7.R3	Address bus	QDR2TOP1_A13	1.5-V HSTL Class I	R18
U7.P8	Address bus	QDR2TOP1_A12	1.5-V HSTL Class I	F18
U7.P7	Address bus	QDR2TOP1_A11	1.5-V HSTL Class I	F17
U7.P5	Address bus	QDR2TOP1_A10	1.5-V HSTL Class I	F16
U7.P4	Address bus	QDR2TOP1_A9	1.5-V HSTL Class I	P18
U7.N7	Address bus	QDR2TOP1_A8	1.5-V HSTL Class I	D17
U7.N6	Address bus	QDR2TOP1_A7	1.5-V HSTL Class I	G18
U7.N5	Address bus	QDR2TOP1_A6	1.5-V HSTL Class I	L19
U7.C7	Address bus	QDR2TOP1_A5	1.5-V HSTL Class I	G19
U7.C5	Address bus	QDR2TOP1_A4	1.5-V HSTL Class I	C18
U7.B8	Address bus	QDR2TOP1_A3	1.5-V HSTL Class I	A18
U7.B4	Address bus	QDR2TOP1_A2	1.5-V HSTL Class I	A17
U7.R8	Address bus	QDR2TOP1_A1	1.5-V HSTL Class I	H19
U7.R9	Address bus	QDR2TOP1_A0	1.5-V HSTL Class I	C17
U7.N2	Write data bus	QDR2TOP1_D17	1.5-V HSTL Class I	G15
U7.M3	Write data bus	QDR2TOP1_D16	1.5-V HSTL Class I	F15
U7.L3	Write data bus	QDR2TOP1_D15	1.5-V HSTL Class I	E16
U7.J3	Write data bus	QDR2TOP1_D14	1.5-V HSTL Class I	D16
U7.G2	Write data bus	QDR2TOP1_D13	1.5-V HSTL Class I	C15
U7.F3	Write data bus	QDR2TOP1_D12	1.5-V HSTL Class I	C16
U7.D2	Write data bus	QDR2TOP1_D11	1.5-V HSTL Class I	B16
U7.C3	Write data bus	QDR2TOP1_D10	1.5-V HSTL Class I	A16
U7.B3	Write data bus	QDR2TOP1_D9	1.5-V HSTL Class I	G16
U7.C11	Write data bus	QDR2TOP1_D8	1.5-V HSTL Class I	G17
U7.D11	Write data bus	QDR2TOP1_D7	1.5-V HSTL Class I	J16
U7.E10	Write data bus	QDR2TOP1_D6	1.5-V HSTL Class I	K16
U7.G11	Write data bus	QDR2TOP1_D5	1.5-V HSTL Class I	L16
U7.J11	Write data bus	QDR2TOP1_D4	1.5-V HSTL Class I	P17
U7.K10	Write data bus	QDR2TOP1_D3	1.5-V HSTL Class I	K17

Table 2–52. QDRII+ Top Port 1 Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U7.M11	Write data bus	QDR2TOP1_D2	1.5-V HSTL Class I	N17
U7.N11	Write data bus	QDR2TOP1_D1	1.5-V HSTL Class I	M17
U7.P10	Write data bus	QDR2TOP1_D0	1.5-V HSTL Class I	P16
U7.B6	Write clock P	QDR2TOP1_K_P	1.5-V HSTL Class I	N16
U7.A6	Write clock N	QDR2TOP1_K_N	1.5-V HSTL Class I	M16
U7.A4	Write port select	QDR2TOP1_WPSn	1.5-V HSTL Class I	D18
U7.B7	Write byte write select 0	QDR2TOP1_BWSn0	1.5-V HSTL Class I	H17
U7.A5	Write byte write select 1	QDR2TOP1_BWSn1	1.5-V HSTL Class I	J17
U7.R6	Termination enable	QDR2TOP1_ODT	1.5-V HSTL Class I	C20
U7.P3	Read data bus	QDR2TOP1_Q17	1.5-V HSTL Class I	N13
U7.N3	Read data bus	QDR2TOP1_Q16	1.5-V HSTL Class I	N15
U7.L2	Read data bus	QDR2TOP1_Q15	1.5-V HSTL Class I	R14
U7.K3	Read data bus	QDR2TOP1_Q14	1.5-V HSTL Class I	P14
U7.G3	Read data bus	QDR2TOP1_Q13	1.5-V HSTL Class I	M14
U7.F2	Read data bus	QDR2TOP1_Q12	1.5-V HSTL Class I	N14
U7.E3	Read data bus	QDR2TOP1_Q11	1.5-V HSTL Class I	M13
U7.D3	Read data bus	QDR2TOP1_Q10	1.5-V HSTL Class I	K14
U7.B2	Read data bus	QDR2TOP1_Q9	1.5-V HSTL Class I	L14
U7.B11	Read data bus	QDR2TOP1_Q8	1.5-V HSTL Class I	E14
U7.C10	Read data bus	QDR2TOP1_Q7	1.5-V HSTL Class I	F14
U7.E11	Read data bus	QDR2TOP1_Q6	1.5-V HSTL Class I	F12
U7.F11	Read data bus	QDR2TOP1_Q5	1.5-V HSTL Class I	G14
U7.J10	Read data bus	QDR2TOP1_Q4	1.5-V HSTL Class I	H14
U7.K11	Read data bus	QDR2TOP1_Q3	1.5-V HSTL Class I	K12
U7.L11	Read data bus	QDR2TOP1_Q2	1.5-V HSTL Class I	J12
U7.M10	Read data bus	QDR2TOP1_Q1	1.5-V HSTL Class I	K13
U7.P11	Read data bus	QDR2TOP1_Q0	1.5-V HSTL Class I	J13
U7.A11	Read clock P	QDR2TOP1_CQ_P	1.5-V HSTL Class I	H13
U7.A1	Read clock N	QDR2TOP1_CQ_N	1.5-V HSTL Class I	L13
U7.A8	Read port select	QDR2TOP1_RPSn	1.5-V HSTL Class I	F19
U7.P6	Read data valid	QDR2TOP1_QVLD	1.5-V HSTL Class I	D13
U7.H1	DLL enable	QDR2TOP1_DOFFn	1.5-V HSTL Class I	D20

Table 2–53 lists the QDRII+ top port 1 component reference and manufacturing information.

Table 2–53. QDRII+ Top Port 1 Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U7	QDRII+, 4 M × 18, 400 MHZ	Cypress	CY7C2563KV18-400BZXC	www.cypress.com
		NEC	uPD44647186AF5-E22-FQ1	www.nec.com
		Samsung	K7S3218U4C-EC40	www.samsung.com

SSRAM

The Synchronous Static Random Access Memory (SSRAM) device consists of a single standard synchronous SRAM, providing 2 MB with a 36-bit data bus. This device is part of the shared FSM Bus, which connects to the flash memory, SSRAM, and the MAX II CPLD EPM2210 System Controller.

The device speed is 250 MHz single-data-rate. There is no minimum speed for this device. The theoretical bandwidth of this 32-bit memory interface is 8.0 Gbps for continuous bursts. The read latency for any address is two clocks, in which at 250 MHz, the latency is 10 ns and at 50 MHz, the latency is 40 ns. The write latency is one clock.

Table 2–54 lists the SSRAM pin assignments, signal names, and functions. The signal names and types are relative to the Stratix IV GX device in terms of I/O setting and direction.

Table 2–54. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U30.P2	Address bus (576 M expansion)	FSM_A25	2.5-V	AP30
U30.C10	Address bus (288 M expansion)	FSM_A24	2.5-V	AN30
U30.B11	Address bus (144 M expansion)	FSM_A23	2.5-V	AL31
U30.A1	Address bus (72 M expansion)	FSM_A22	2.5-V	AK31
U30.B1	Address bus (36 M expansion)	FSM_A21	2.5-V	AR32
U30.R11	Address bus	FSM_A20	2.5-V	AP32
U30.R10	Address bus	FSM_A19	2.5-V	AH29
U30.R9	Address bus	FSM_A18	2.5-V	AG29
U30.R8	Address bus	FSM_A17	2.5-V	AR35
U30.R4	Address bus	FSM_A16	2.5-V	AP35
U30.R3	Address bus	FSM_A15	2.5-V	AL32
U30.P11	Address bus	FSM_A14	2.5-V	AK32
U30.P10	Address bus	FSM_A13	2.5-V	AU33
U30.P9	Address bus	FSM_A12	2.5-V	AT33
U30.P8	Address bus	FSM_A11	2.5-V	AH30
U30.P4	Address bus	FSM_A10	2.5-V	AJ31
U30.P3	Address bus	FSM_A9	2.5-V	AR34

Table 2–54. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U30.N6	Address bus	FSM_A8	2.5-V	AT34
U30.B10	Address bus	FSM_A7	2.5-V	AE27
U30.B2	Address bus	FSM_A6	2.5-V	AD27
U30.A10	Address bus	FSM_A5	2.5-V	AP34
U30.A2	Address bus	FSM_A4	2.5-V	AN33
U30.P6	Address bus	FSM_A3	2.5-V	AD26
U30.R6	Address bus	FSM_A2	2.5-V	AC26
U30.M2	Data bus	FSM_D31	2.5-V	T28
U30.M1	Data bus	FSM_D30	2.5-V	R28
U30.L2	Data bus	FSM_D29	2.5-V	F32
U30.L1	Data bus	FSM_D28	2.5-V	E32
U30.K2	Data bus	FSM_D27	2.5-V	L31
U30.K1	Data bus	FSM_D26	2.5-V	K31
U30.J2	Data bus	FSM_D25	2.5-V	F31
U30.J1	Data bus	FSM_D24	2.5-V	E31
U30.G2	Data bus	FSM_D23	2.5-V	N29
U30.G1	Data bus	FSM_D22	2.5-V	M29
U30.F2	Data bus	FSM_D21	2.5-V	H31
U30.F1	Data bus	FSM_D20	2.5-V	G31
U30.E2	Data bus	FSM_D19	2.5-V	N30
U30.E1	Data bus	FSM_D18	2.5-V	M30
U30.D2	Data bus	FSM_D17	2.5-V	D33
U30.D1	Data bus	FSM_D16	2.5-V	C33
U30.G11	Data bus	FSM_D15	2.5-V	N31
U30.G10	Data bus	FSM_D14	2.5-V	M31
U30.F11	Data bus	FSM_D13	2.5-V	C32
U30.F10	Data bus	FSM_D12	2.5-V	B32
U30.E11	Data bus	FSM_D11	2.5-V	J32
U30.E10	Data bus	FSM_D10	2.5-V	H32
U30.D11	Data bus	FSM_D9	2.5-V	D35
U30.D10	Data bus	FSM_D8	2.5-V	C35
U30.M11	Data bus	FSM_D7	2.5-V	N28
U30.M10	Data bus	FSM_D6	2.5-V	M28
U30.L11	Data bus	FSM_D5	2.5-V	D31
U30.L10	Data bus	FSM_D4	2.5-V	C31
U30.K11	Data bus	FSM_D3	2.5-V	K30
U30.K10	Data bus	FSM_D2	2.5-V	J30
U30.J11	Data bus	FSM_D1	2.5-V	D34
U30.J10	Data bus	FSM_D0	2.5-V	C34

Table 2–54. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U30.N11	Data bus parity byte lane 0	SRAM_DQP0	2.5-V	F35
U30.C11	Data bus parity byte lane 1	SRAM_DQP1	2.5-V	AJ32
U30.C1	Data bus parity byte lane 2	SRAM_DQP2	2.5-V	N33
U30.N1	Data bus parity byte lane 3	SRAM_DQP3	2.5-V	AJ35
U30.B6	Clock	SRAM_CLK	2.5-V	AE26
U30.B8	Output enable	SRAM_OEn	2.5-V	AK34
U30.A3	Chip enable	SRAM_CEn	2.5-V	AT30
U30.B5	Byte lane 0 write enable	SRAM_BWn0	2.5-V	AH27
U30.A5	Byte lane 1 write enable	SRAM_BWn1	2.5-V	AR31
U30.A4	Byte lane 2 write enable	SRAM_BWn2	2.5-V	AH28
U30.B4	Byte lane 3 write enable	SRAM_BWn3	2.5-V	AL29
U30.A7	Byte write enable	SRAM_BWEn	2.5-V	AK30
U30.B7	Global write enable	SRAM_GWn	2.5-V	AC29
U30.A8	Address status controller	SRAM_ADSCn	2.5-V	AM31
U30.B9	Address status processor	SRAM_ADSPn	2.5-V	AG28
U30.A9	Address valid	SRAM_ADVn	2.5-V	AU32
U30.R1	Mode	SRAM_MODE	2.5-V	— (Connects to the MAX II CPLD EPM2210 System Controller)
U30.H11	Sleep	SRAM_ZZ	2.5-V	AJ29

Table 2–55 lists the SSRAM component reference and manufacturing information.

Table 2–55. SSRAM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U30	Standard synchronous pipelined SCD, 512K × 36 bit, 250 MHz	ISSI Inc.	IS61VPS51236A-250B3	www.issi.com

Flash

The flash interface consists of a single synchronous flash memory device, providing 64 MB interface with a 16-bit data bus. This device is part of the shared FSM Bus, which connects to flash memory, SSRAM, and the Max II CPLD EPM2210 System Controller.

There are two 256 MB die per package with A(25) low selecting the lower die and A(25) high selecting the upper die. Parameter blocks are 32 K and main blocks are 128 K. The parameters of this device are located at both the top and bottom of the address space.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps. The write performance is 125 µs for a single word and 440 µs for a 32-word buffer. The erase time is 400 ms for a 32 K parameter block and 1200 ms for a 128 K main block.

Table 2–56 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Stratix IV GX device in terms of I/O setting and direction.

Table 2–56. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U32.B6	Address bus (die select)	FSM_A25	2.5-V	AP30
U32.H8	Address bus	FSM_A24	2.5-V	AN30
U32.G1	Address bus	FSM_A23	2.5-V	AL31
U32.A8	Address bus	FSM_A22	2.5-V	AK31
U32.C8	Address bus	FSM_A21	2.5-V	AR32
U32.C7	Address bus	FSM_A20	2.5-V	AP32
U32.B7	Address bus	FSM_A19	2.5-V	AH29
U32.A7	Address bus	FSM_A18	2.5-V	AG29
U32.D8	Address bus	FSM_A17	2.5-V	AR35
U32.D7	Address bus	FSM_A16	2.5-V	AP35
U32.C5	Address bus	FSM_A15	2.5-V	AL32
U32.B5	Address bus	FSM_A14	2.5-V	AK32
U32.A5	Address bus	FSM_A13	2.5-V	AU33
U32.C4	Address bus	FSM_A12	2.5-V	AT33
U32.D3	Address bus	FSM_A11	2.5-V	AH30
U32.C3	Address bus	FSM_A10	2.5-V	AJ31
U32.B3	Address bus	FSM_A9	2.5-V	AR34
U32.A3	Address bus	FSM_A8	2.5-V	AT34
U32.C2	Address bus	FSM_A7	2.5-V	AE27
U32.A2	Address bus	FSM_A6	2.5-V	AD27
U32.D2	Address bus	FSM_A5	2.5-V	AP34
U32.D1	Address bus	FSM_A4	2.5-V	AN33
U32.C1	Address bus	FSM_A3	2.5-V	AD26
U32.B1	Address bus	FSM_A2	2.5-V	AC26
U32.A1	Address bus	FSM_A1	2.5-V	AP33
U32.E7	Data bus	FSM_D16	2.5-V	C33
U32.G7	Data bus	FSM_D15	2.5-V	N31
U32.H5	Data bus	FSM_D14	2.5-V	M31
U32.F5	Data bus	FSM_D13	2.5-V	C32
U32.F4	Data bus	FSM_D12	2.5-V	B32
U32.F3	Data bus	FSM_D11	2.5-V	J32

Table 2–56. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV GX Device Pin Number
U32.E3	Data bus	FSM_D10	2.5-V	H32
U32.E1	Data bus	FSM_D9	2.5-V	D35
U32.H7	Data bus	FSM_D8	2.5-V	C35
U32.G6	Data bus	FSM_D7	2.5-V	N28
U32.G5	Data bus	FSM_D6	2.5-V	M28
U32.E5	Data bus	FSM_D5	2.5-V	D31
U32.E4	Data bus	FSM_D4	2.5-V	C31
U32.G3	Data bus	FSM_D3	2.5-V	K30
U32.E2	Data bus	FSM_D2	2.5-V	J30
U32.F2	Data bus	FSM_D1	2.5-V	D34
U32.E6	Data bus	FSM_D0	2.5-V	C34
U32.D4	Clock	FLASH_CLK	2.5-V	AF26
U32.B4	Reset	FLASH_RESETn	2.5-V	AL30
U32.F8	Chip enable	FLASH_CEn	2.5-V	AU31
U32.G8	Output enable	FLASH_OEn	2.5-V	AG27
U32.F6	Address valid	FLASH_ADVn	2.5-V	AN31
U32.F7	Ready	FLASH_RDYBSYn	2.5-V	AT32

Table 2–57 lists the flash memory component reference and manufacturing information.

Table 2–57. Flash Memory Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U32	512-MB synchronous flash	Numonyx	PC28F512P30BF	www.numonyx.com

Power Supply

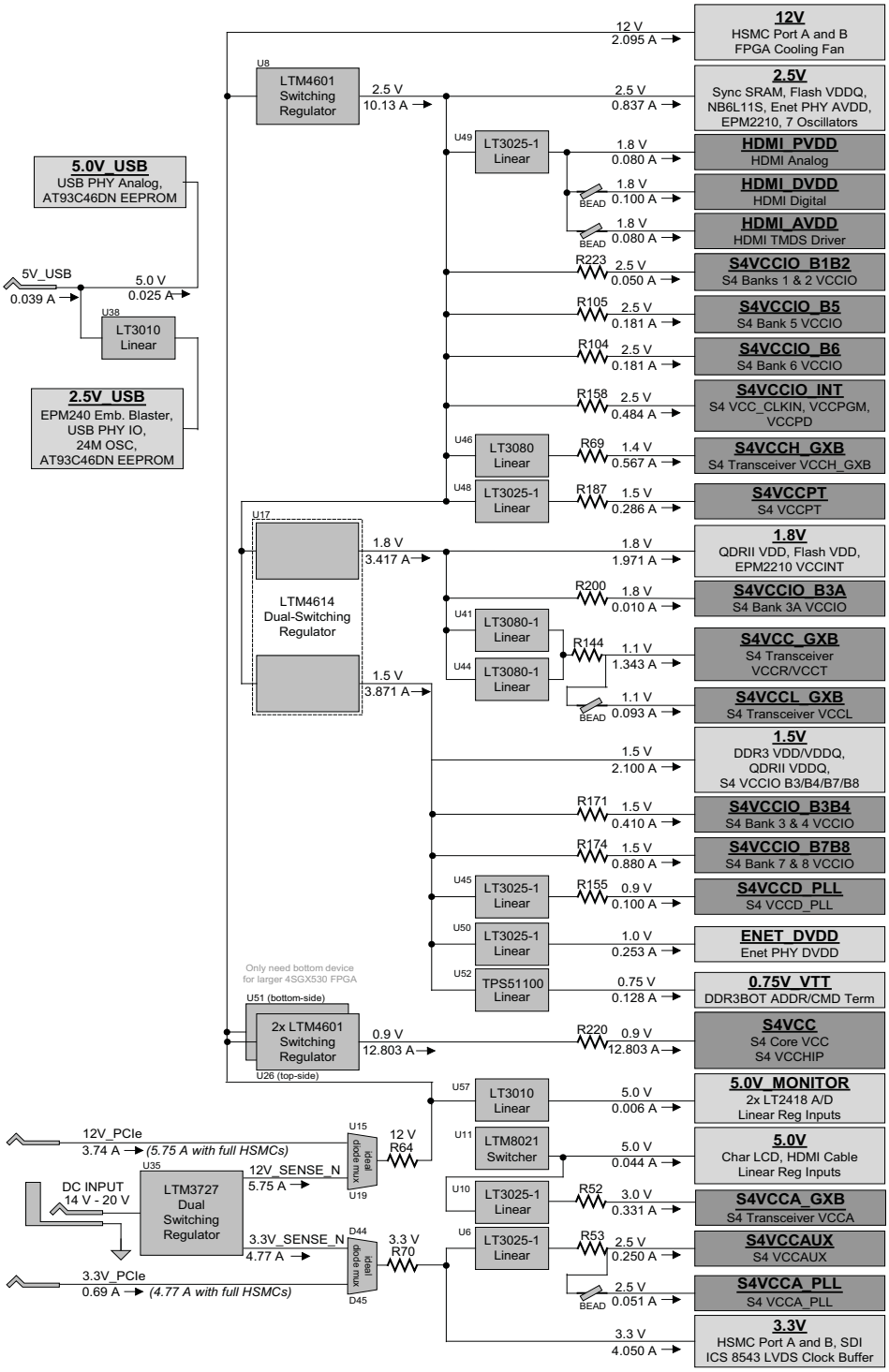
The development board's power is provided through a laptop style DC power input. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to the various power rails used by the components on the board and installed into the HSMC connectors.

An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed in a GUI that graphs power consumption versus time.

Power Distribution System

Figure 2–15 shows the power distribution system on the development board. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

Figure 2–15. Power Distribution System



Power Measurement

There are 16 power supply rails that have on-board voltage and current sense capabilities. These 8-channel differential 24-bit ADC devices and rails are split from the primary supply plane by a low-value sense resistor for the ADC to measure voltage and current. A serial peripheral interface (SPI) bus connects these ADC devices to the MAX II CPLD EPM2210 System Controller as well as the Stratix IV GX FPGA.

Figure 2–16 shows the block diagram for the power measurement circuitry.

Figure 2–16. Power Measurement Circuit

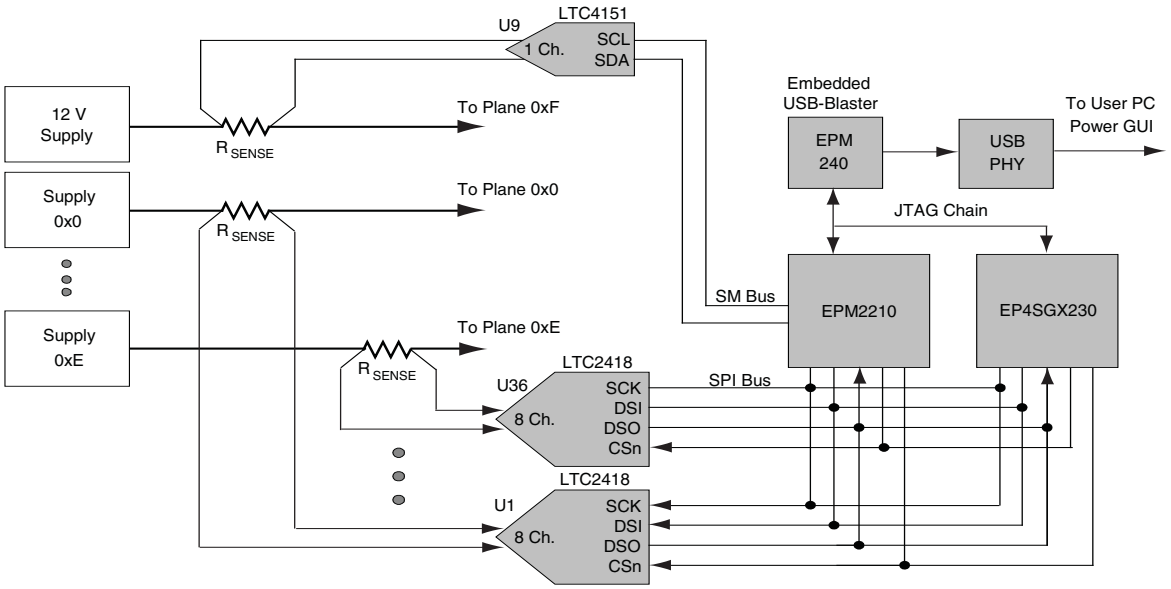


Table 2–58 lists the targeted rails. The schematic signal name specifies the name of the rail being measured and the device pin specifies the devices attached to the rail. If no subnet is named, the power is the total output power for that voltage.

Table 2–58. Power Rail Measurements Based on the Rotary Switch Position (Part 1 of 2) (1)

Switch	Schematic Signal Name	Voltage (V)	Device Pin	Description
0	S4VCCIO_B7B8	1.5	VCCIO_B7	Bank 7 I/O power (QDR2TOP+DDR3TOP)
			VCCIO_B8	Bank 8 I/O power (QDR2TOP+DDR3TOP)
1	S4VCC	0.9	VCC	FPGA core and periphery power
			VCCHIP	PCI Express hard IP block
2	3.3 V	3.3	—	All 3.3 V power to board (mA only)
3	S4VCCIO_INT	2.5	VCCPD	I/O pre-drivers
			VCCPGM	Configuration I/O
			VCC_CLKIN	V_{IO} clock input pins
4	S4VCCH_GXB	1.4	VCCH_GXB	XCVR clock buffers
5	S4VCCAUX	2.5	VCCAUX	Programmable power tech auxiliary
			VCCA_PLL	PLL analog

Table 2–58. Power Rail Measurements Based on the Rotary Switch Position (Part 2 of 2) (1)

Switch	Schematic Signal Name	Voltage (V)	Device Pin	Description
6	S4VCCPT	1.5	VCCPT	Programmable power tech
7	S4VCCD_PLL	0.9	VCCD_PLL	PLL digital
8	S4VCCA_GXB	3.0	VCCA	XCVR analog TX/RX driver (mA only)
9	S4VCCIO_B5	2.5	VCCIO_B5	Bank 5 I/O power (HSMC port A)
A	S4VCCIO_B6	2.5	VCCIO_B6	Bank 6 I/O power (HSMC port B)
B	S4VCCIO_B1B2	2.5	VCCIO_B1	Bank 1 I/O power (FSM bus)
			VCCIO_B2	Bank 2 I/O power (FSM bus)
C	S4VCCIO_B3A	1.8	VCCIO_B3A	Bank 3A I/O power (HDMI)
D	S4VCCIO_B3B4	1.5	VCCIO_B3	Bank 3 I/O power (DDR3BOT)
			VCCIO_B4	Bank 4 I/O power (DDR3BOT)
E	S4VCC_GXB	1.1	VCCR	XCVR analog receive
			VCCT	XCVR analog transmit
			VCCL_GXB	XCVR clock distribution
F	—	—	—	—

Note for Table 2–58:

(1) The targeted power rails whose voltage values on the engineering silicon board differ from the production silicon board are listed in Table A–2 on page A–2.

Table 2–59 lists the power measurement ADC component references and manufacturing information.

Table 2–59. Power Measurement ADC Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U1, U36	8-channel differential 24-bit ADC	Linear Technology	LTC2418CGN#PBF	www.linear.com
U9	1-channel differential 12-bit ADC	Linear Technology	LTC4151CDD#PBF	www.linear.com

Temperature Sense

Temperature monitoring for the Stratix IV GX FPGA die is achieved with a MAX1619 temperature sense device. The MAX1619 device connects to the MAX II CPLD EPM2210 System Controller and the Stratix IV GX device by a 2-wire SMB interface. The MAX 1619 device is located at address 0x1. This bus also routes to a single voltage and power monitor chip for the 12-V power rail at address 0x2.

The OVERTEMPn and TSENSE_ALERTn signals are driven by the MAX1619 temperature sense device based on a programmable threshold temperature. The OVERTEMPn signal is driven to the MAX II EPM2210 System Controller. When the OVERTEMPn signal goes high, the on-board fan is enabled. The MAX II EPM2210 System Controller can control fan speed based on a register setting and can also override the MAX1619 device with the FAN_FORCE_ON DIP switch to force the fan to be on constantly at full speed. For more information on this control, refer to the MAX II EPM2210 System Controller source code found in the development board installation directory *<install dir>***stratixIVGX_4sgx230_fpga \examples\max2**.

For more information on the development board installation directory, refer to the *Stratix IV GX FPGA Development Kit User Guide*.

The remote sense routes to the FPGA diode pins to measure the voltage drop. For very accurate temperature readings, the I/O adjacent to the FPGA diode sense pins must be halted.

Table 2–60 lists the temperature sense interface pin assignments, signal names, and functions.

Table 2–60. Temperature Sense Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX II CPLD EPM2210 System Controller Pin Number	Stratix IV GX Device Pin Number
U27.14	SMB clock	SENSE_SMB_CLK	2.5-V	R1	W34
U27.12	SMB data	SENSE_SMB_DATA	2.5-V	R4	AH32
U27.9	Programmable over-temperature	OVERTEMPn	2.5-V	P5	—
U27.11	Programmable alert	TSENSE_ALERTn	2.5-V	M2	—

Table 2–61 lists the temperature sense component reference and manufacturing information.

Table 2–61. Temperature Sense Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U26	Temperature sense, remote and local, programmable alert.	Maxim	MAX1619MEE+T	www.maxim-ic.com

Statement of China-RoHS Compliance

Table 2–62 lists hazardous substances included with the kit.

Table 2–62. Table of Hazardous Substances' Name and Concentration ***Notes*** **(1), (2)**

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Stratix IV GX development board	X*	0	0	0	0	0
12 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–62:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

A. Board Revision History

This appendix catalogs revisions to the Stratix IV GX FPGA development board.

Table A–1 lists the versions of all releases of the Stratix IV GX FPGA development board.

Table A–1. Stratix IV GX FPGA Development Board Revision History

Version	Release Date	Description
Single-die flash	June 2010	■ Replaced Intel dual-die 512-Mb flash PC48F4400P0VB00 with Numonyx single-die flash PC28F512P30BF.
Production silicon	November 2009	■ New MAX II CPLD EPM2210 System Controller design. ■ New voltage values for the power rails measurement. ■ Replaced 100-MHz fixed frequency oscillator (X6) with a programmable oscillator described in clocking section.
Engineering silicon	May 2009	Initial release.

Single-Die Flash Version Differences

The single-die flash version of the Stratix IV GX FPGA development board is created to replace the obsolete dual-die flash device with a single-die flash device. The two flash devices are considered equivalent except for some software routines used to access them because the single-die device has only one CFI table whereas the duel-die device has two CFI tables.

To determine which flash your board is using, refer to the device part number installed at U32. The single-die package is smaller than the dual-die version.

For more information about the flash change and its application, refer to the *Stratix IV GX FPGA Development Kit User Guide*.

Engineering Silicon Version Differences

The engineering silicon version of the Stratix IV GX FPGA development board is the initial release of the board. This section describes the differences between the engineering silicon and production silicon versions of the board.

Figure A–1 illustrates the Max II CPLD EPM2210 System Controller block diagram whose functionality and external circuit connections on the engineering silicon board differ from the production silicon board. Figure 2–3 on page 2–8 shows the production silicon MAX II CPLD EPM2210 System Controller block diagram.

Figure A–1. MAX II CPLD EPM2210 System Controller Block Diagram

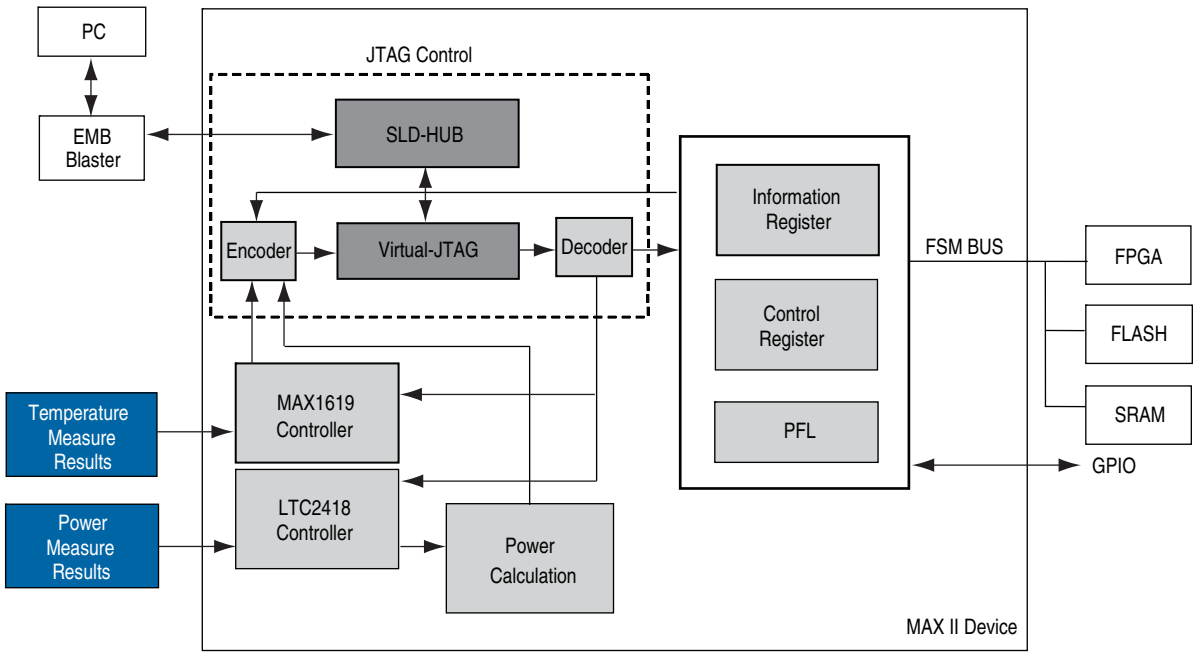


Table A–2 lists information for the targeted power rails whose voltage values on the engineering silicon board differ from the production silicon board. Table 2–58 on page 2–64 shows the production silicon voltage values.

Table A–2. Power Rail Measurements that Differ on the Engineering Silicon Board

Switch	Schematic Signal Name	Voltage (V)	Device Pin	Description
1	S4VCC	0.95	VCC	FPGA core and periphery power
			VCCHIP	PCI Express hard IP block
7	S4VCCD_PLL	0.95	VCCD_PLL	PLL digital
8	S4VCCA_GXB	3.3	VCCA	XCVR analog TX/RX driver (mA only)
E	S4VCC_GXB	1.2	VCCR	XCVR analog receive
			VCCT	XCVR analog transmit
			VCCL_GXB	XCVR clock distribution

The engineering silicon version does not have the programmable oscillator supported for reference designator X6 but has a fixed frequency 100-MHz oscillator from Epson. The engineering silicon board version works with the new programmable oscillator if you remove the Epson device and install it. The latest MAX II CPLD EPM2210 System Controller also works with older board versions.

Table A–3 lists the crystal oscillators whose component reference and manufacturing information on the engineering silicon board differ from the production silicon board. Table 2–22 on page 2–26 shows the production silicon component references.

Table A–3. Crystal Oscillator Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
X6	100 MHz LVDS Saw Oscillator	Epson	EG-2121CA 100.0000M-LHPNL3	www.eea.epson.com

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
August 2012	2.3	■ Corrected the schematic signal names for board references J2.108 and J2.109 in Table 2–38. ■ Added DDR3BOT_RSTn signal in Table 2–46. ■ Added DDR3TOP_RSTn signal in Table 2–48. ■ Maintenance release.
August 2010	2.2	■ Updated the manufacturing part number of the flash device in Table 2–57. ■ Converted document to new frame template and made textual and style changes.
June 2010	2.1	■ Updated Stratix IV GX FPGA development board block diagram in Figure 1–1. ■ Updated the description of the HDMI video port (J11) in Table 2–1, and in "HDMI Video Output" on page 2–42. ■ Updated the manufacturing part number of the Stratix IV GX device in Table 2–3. ■ Added "Single-Die Flash Version Differences" on page A–1 to document the replacement of dual-die 512-Mb flash with a single-die flash device.
November 2009	2.0	■ Updated MAX II CPLD EPM2210 System Controller block diagram in Figure 2–3. ■ Added two I/O signals, CLK100_SDA and CLK100_SCL in Table 2–6. ■ Replaced 100-MHz fixed frequency oscillator (X6) with a programmable oscillator described in clocking section. ■ Increased SRAM frequency to 250 MHz. ■ Corrected schematic signal names in Table 2–46 and Table 2–48. ■ Added manufacturing information for QDRII+ top port 1 SRAM memory in Table 2–51 and Table 2–53. ■ Updated voltage values for the power rails measurement in Table 2–58. ■ Updated power distribution system in Figure 2–15. ■ Added an appendix to document the board revision change (engineering silicon to production silicon revisions).
August 2009	1.3	■ Corrected DDR3 top port schematic signal names in Table 2–48.
July 2009	1.2	■ Added HSMA present LED and HSMB present LED board components, and corrected SSRAM x36 Memory description in Table 2–1. ■ Updated I/O count in Table 2–4. ■ Corrected PCI Express edge description in Table 2–20. ■ Corrected LVDS schematic signal names in Table 2–37 and Table 2–38.

Date	Version	Changes
May 2009	1.1	■ Updated board component blocks list. ■ Updated development board block diagram Figure 1–1.
May 2009	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.