A product Line of
Diodes Incorporated

**PI3EQX1001**

**1-Channel USB3.1 GEN-2 ReDriver**

## Features

- 5 & 10Gbps serial link with linear equalizer.
- USB3.1 and USB3.0 Compatible
- Full Compliancy to USB3.1 Super Speed Standard
- Single 10Gbps differential signal pairs
- Pin Adjustable Receiver Equalization
- Pin Adjustable Flat Gain
- 100Ω Differential CML I/O's
- Automatic Receiver Detect
- Auto "Slumber" mode for adaptive power management
- Single Supply Voltage: 3.3V
- Packaging:
  - 18-pin, X2QFN 2x2 mm (XUA18)

## Description

The PI3EQX1001 is a low power, high performance 10.0 Gbps 1-Channel USB 3.1 linear ReDriver™ designed specifically for the USB 3.1 protocol.

The device provides programmable equalization, and flat gain to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX1001 supports one 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. The channels' input signal level determines whether the output is active.

The PI3EQX1001 also includes an automatic receiver detect function. The receiver detection loop will be active again if the corresponding channel's signal detector is idle for longer than 7.3mS. The channel will then move to Unplug Mode if load not detected, or it will return to Low Power Mode (Slumber Mode) due to inactivity.

## Block Diagram

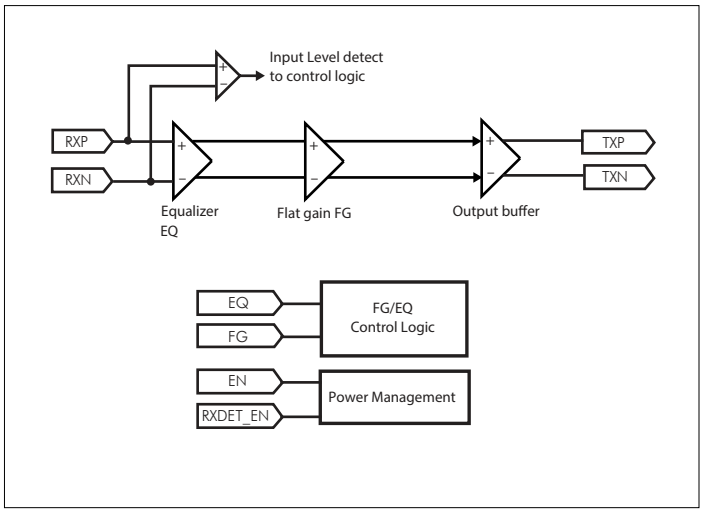
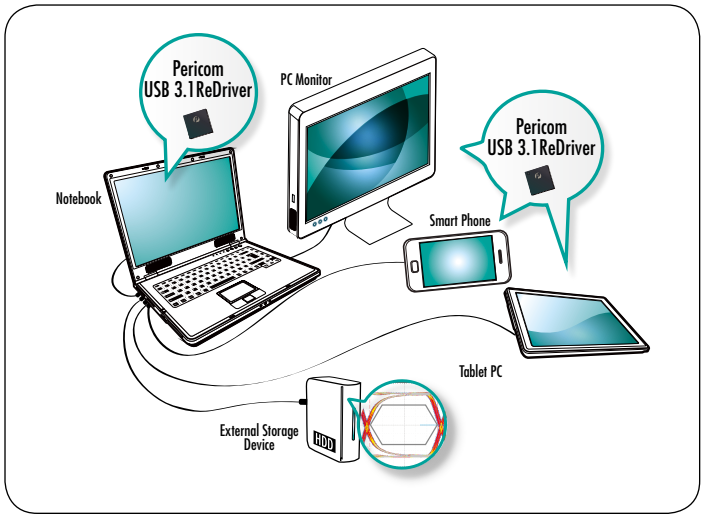
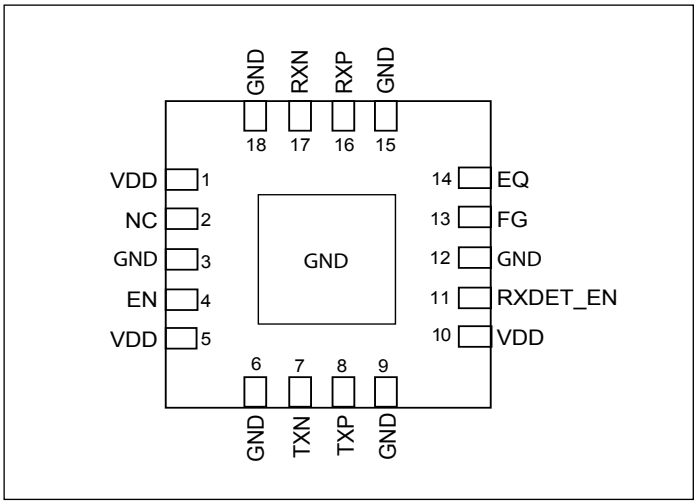



**Figure1**



### Pin Diagram (18-pin, X2QFN 2x2mm) XUA18




## Pin Description

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1, 5, 10 | VDD | Power | 3.3V power supply, +/-0.3V |
| 13 | FG | Input | The DC flat gain selection. 4-level input pins. With internal 100KΩ pull-up resistor and 200kΩ pull-down resistor. |
| 14 | EQ | Input | The EQ selection. 4-level input pins. With internal 100KΩ pull-up resistor and 200kΩ pull-down resistor. |
| 16, 17 | RXP, RXN | Input | CML input terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. |
| 8, 7 | TXP, TXN | Output | CML output terminals. With selectable output termination between 50Ω to VDD, 4K to VDD, 4K to VbiasTx or Hi-Z |
| 11 | RXDET_EN | Input | Receiver detection Enable pin. With internal 300kΩ pull-up resistor.<br>"High" – Receiver detection is enabled.<br>"Low" – Receiver detection is disabled. |
| 4 | EN | Input | Channel Enable. With internal 300kΩ pull-up resistor.<br>"High" – Channel is in normal operation.<br>"Low" – Channel is in power down mode. |
| 3, 6, 9, 12, 15, 18, Center Pad | GND | GND | Supply Ground |
| 2 | NC | NC | No Connect |

## Power Management

Notebooks, netbooks, and other power sensitive consumer devices require judicious use of power in order to maximize battery life. In order to minimize the power consumption of our devices, Diodes has added an additional adaptive power management feature. When a signal detector is idle for longer than 1.3ms, the corresponding channel will move to low power mode ONLY. (It means both channels will move to low power mode individually).

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in low power mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. If load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuously. If load is detected, it will return to Low Power Mode and receiver detection will be active again per 6ms.

## Operating Modes

| Mode | $R_{IN}$ | $R_{OUT}$ |
|---|---|---|
| PD | 67KΩ to GND | HIZ |
| Unplug Mode | 67KΩ to VbiasRx | 4KΩ to VbiasTx |
| Deep Slumber Mode | 50Ω to Vdd | 4KΩ to VbiasTx |
| Slumber Mode | 50Ω to Vdd | 4KΩ to Vdd |
| Active Mode | 50Ω to Vdd | 50Ω to Vdd |

## Equalization Setting:

EQ is the selection pin for the equalization selection

| | Equalizer setting (dB) | |
|---|---|---|
| *EQ* | *@2.5GHz* | *@5GHz* |
| 0 (Tie 0Ω to GND) | 5.1 | 10.9 |
| R (Tie Rext to Gnd) | 1.9 | 6.7 |
| F (Leave Open) | 3.5 | 8.9 (Default) |
| 1 (Tie 0Ω to VDD) | 6.8 | 13.1 |

## Flat Gain Setting:

FG is the selection pin for the DC gain

| | Flat Gain Settings |
|---|---|
| *FG* | *dB* |
| 0 (Tie 0Ω to GND) | -3 |
| R (Tie Rext to Gnd) | -1.5 |
| F (Leave Open) | 0 (Default) |
| 1 (Tie 0Ω to VDD) | +2 |

## Channel Enable Setting:

EN is the channel enable pin

| | Channel Enable Setting |
|---|---|
| *EN* | *Setting* |
| 0 | Disabled |
| 1 | Enabled (Default) |

## Receiver Detection Setting:

RXDET_EN is the receiver detection pin

| | Receiver Detection Setting |
|---|---|
| *RXDET_EN* | *Setting* |
| 0 | Disabled |
| 1 | Enabled (Default) |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential ..... –0.5V to +4.6V
DC SIG Voltage ..... –0.5V to $V_{DD}$ +0.5V
Output Current ..... –25mA to +25mA
Power Dissipation Continuous ..... 0.5W
ESD, Human Body Model ..... -2kV to +2kV

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Control pin Specifications (VDD = 3.3 ± 0.3V TA = 0 to 70°C)

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **2-level control pins** | | | | | |
| $V_{IH}$ | DC input logic High | VDD*0.65 | | | V |
| $V_{IL}$ | DC input logic Low | | | VDD*0.35 | V |
| $I_{IH}$ | Input High current | | | 25 | uA |
| $I_{IL}$ | Input Low current | -25 | | | uA |
| **4-level control pins** | | | | | |
| $V_{IH}$ | DC input logic "High" | 0.92*VDD | VDD | | V |
| $V_{IF}$ | DC input logic "Float" | 0.59*VDD | 0.67*VDD | 0.75*VDD | V |
| $V_{IR}$ | DC input logic "With Rext to GND" | 0.25*VDD | 0.33*VDD | 0.41*VDD | V |
| $V_{IL}$ | DC input logic "Low" | | GND | 0.08*VDD | V |
| $I_{IH}$ | Input High current | | | 50 | uA |
| $I_{IL}$ | Input Low current | -50 | | | uA |
| Rext | External resistor connects to GND (±5%) | 64.6 | 68 | 71.4 | kΩ |

## AC/DC Electrical Characteristics (VDD = 3.3 ± 0.3V TA = 0 to 70°C)

| **Power and Latency** | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Units** |
| $V_{dd-3.3}$ | Supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $I_{active}$ | Active mode current consumption | EN=1 (VDD=3.3V, 10Gbps, compliance test pattern, $_{RXDET\_EN}$=High) | | 65 | 88 | mA |
| $I_{slumber}$ | Slumber mode current consumption | EN=1 (VDD=3.3V, no input signal longer than $T_{slumber}$ /RXDET_EN=High) | | 8 | 11 | mA |
| $I_{DeepSlumber}$ | Deep slumber mode current consumption | EN=1 (VDD=3.3V, no input signal longer than $T_{DeepSlumber}$/ RXDET_EN=High) | | 0.4 | 0.7 | |
| $I_{unplug}$ | Unplug mode current consumption | EN=1, no output load is detected | | 0.3 | 0.5 | |
| $I_{pd}$ | Power Down mode current consumption | EN=0 | | 10 | 50 | µA |
| $t_{pd}$ | Latency | From input to output | | | 2 | ns |

## AC/DC Electrical Characteristics Cont.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **CML Receiver Input (100Ω differential)** | | | | | | |
| Receiver Electrical Specification | | | | | | |
| $C_{rxparasitic}$ | The parasitic capacitor for RX | | | | 1.0 | pF |
| $R_{RX-DIFF-DC}$ | DC Differential Input Impedance | | 72 | | 120 | Ω |
| $R_{RX-SINGLE\_DC}$ | DC single ended input impedance | DC impedance limits are need to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max | 18 | | 30 | Ω |
| $Z_{RX-HIZ-DC-PD}$ | DC input CM input impedance for V>0 during reset or power down | (Vcm=0 to 500mV) | 25 | | | kΩ |
| $C_{ac\_coupling}$ | AC coupling capacitance | | 75 | | 265 | nF |
| $V_{RX-CM-AC-P}$ | Common mode peak voltage | AC up to 5GHz | | | 150 | mV-peak |
| $V_{RX-CM-DC-Active-Idle-Delta-P}$ | Common mode peak voltage $\lvert Avg_{u0}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2 - Avg_{u1}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2\rvert$ | Between U0 and U1. AC up to 5GHz | | | 200 | mV-peak |
| Transmitter Electrical Specification | | | | | | |
| $V_{TX-DIFF-PP}$ | Ouput differential p-p voltage swing | Differential Swing $\lvert V_{TX-D+} - V_{TX-D-}\rvert$ | | | 1.2 | Vppd |
| $R_{TX-DIFF-DC}$ | DC Differential TX Impedance | | 72 | | 120 | Ω |
| $V_{TX-RCV-DET}$ | The amount of voltage change allowed during RxDet | | | | 600 | mV |
| $C_{ac\_coupling}$ | AC coupling capacitance | | 75 | | 265 | nF |
| $T_{TX-EYE(10Gbps)}$ | Transmitter eye, Include all jittter | At the silicon pad. 10Gbps | 0.646 | | | UI |
| $T_{TX-EYE(5Gbps)}$ | Transmitter eye, Include all jittter | At the silicon pad. 5Gbps | 0.625 | | | UI |
| $T_{TX-DJ-DD(10Gbps)}$ | Transmitter deterministic jittter | At the silicon pad. 10Gbps | | | 0.17 | UI |
| $T_{TX-DJ-DD(5Gbps)}$ | Transmitter deterministic jittter | At the silicon pad. 5Gbps | | | 0.205 | UI |
| $C_{txparasitic}$ | The parasitic capacitor for TX | | | | 1.1 | pF |
| $R_{TX-DC-CM}$ | Common mode DC output Impedance | | 18 | | 30 | Ω |
| $V_{TX-DC-CM}$ | The instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors | $\lvert V_{TX-D+} + V_{TX-D-}\rvert/2$ | 0 | | 2.2 | V |
| $V_{TX-C}$ | Common-Mode Voltage | $\lvert V_{TX-D+} + V_{TX-D-}\rvert/2$ | VDD-1.5V | | VDD | V |
| $V_{TX-CM-AC-PP-Active}$ | Active mode TX AC common mode voltage | $V_{TX-D+} + V_{TX-D-}$ for both time and amplitude | | | 100 | mVpp |

## AC/DC Electrical Characteristics Cont.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{TX-CM-DC-Active\_Idle-Delta}$ | Common mode delta voltage $\lvert Avg_{uo}(\lvert V_{TEX-D+} + V_{TX-D-}\rvert)/2 - Avg_{u1}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2\rvert$ | Between U0 to U1 | | | 200 | mV-peak |
| $V_{TX-Idle-Diff-AC-pp}$ | Idle mode AC common mode delta voltage$\lvert V_{TX-D+}-V_{TX-D-}\rvert$ | Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals . | | | 10 | mVppd |
| $V_{TX-Idle-Diff-DC}$ | Idle mode DC common mode delta voltage$\lvert V_{TX-D+}-V_{TX-D-}\rvert$ | Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals. | | | 10 | mV |
| Channel Performance | | | | | | |
| $G_p$ | Peaking gain (Compensation at 5GHz, relative to 100MHz, 100$mV_{p-p}$ sine wave input, FG=F) | EQ=0<br>EQ=R<br>EQ=F<br>EQ=1 | | 10.9<br>6.7<br>8.9<br>13.1 | | dB |
| | | Variation around typical | -3 | | +3 | dB |
| $G_F$ | Flat gain (100MHz, EQ=F) | FG=0<br>FG=R<br>FG=F<br>FG=1 | | -3<br>-1.5<br>0<br>+2 | | dB |
| | | Variation around typical | -3 | | +3 | dB |
| $V_{SW\_100M}$ | -1dB compression point output swing (at 100MHz) | | | 1000 | | mVppd |
| $V_{SW\_5G}$ | -1dB compression point output swing (at 5GHz) | | | 750 | | mVppd |
| $V_{noise-input}$ | Input-referred noise | 100MHz to 5GHz, FG=1, EQ=R, Figure 2 | | 0.6 | | $mV_{RMS}$ |
| | | 100MHz to 5GHz, FG=1, EQ=1, Figure 2 | | 0.5 | | |
| $V_{noise-output}$ | Output-referred noise[1] | 100MHz to 5GHz, FG=1, EQ=R, Figure 2 | | 0.8 | | $mV_{RMS}$ |
| | | 100MHz to 5GHz, FG=1, EQ=1, Figure 2 | | 1 | | |
| Signal and Frequency Detectors | | | | | | |
| $V_{th\_upm}$ | Unplug mode detector threshold | Threshold of LFPS when the input impedance of the redriver is 67kohm to VbiasRx only. Used in the unplug mode. | 200 | | 800 | mVppd |
| $V_{th\_dsm}$ | Deep slumber mode detector threshold | LFPS signal threshold in Deep slumber mode | 100 | | 600 | mVppd |
| $V_{th\_am}$ | Active mode detector threshold | Signal threshold in Active and slumber mode | 45 | | 175 | mVppd |
| $F_{th}$ | LFPS frequency detector | Detect the frequency of the input CLK pattern | 100 | | 400 | MHz |

**Note:** 1. Guaranteed by design and characterization.

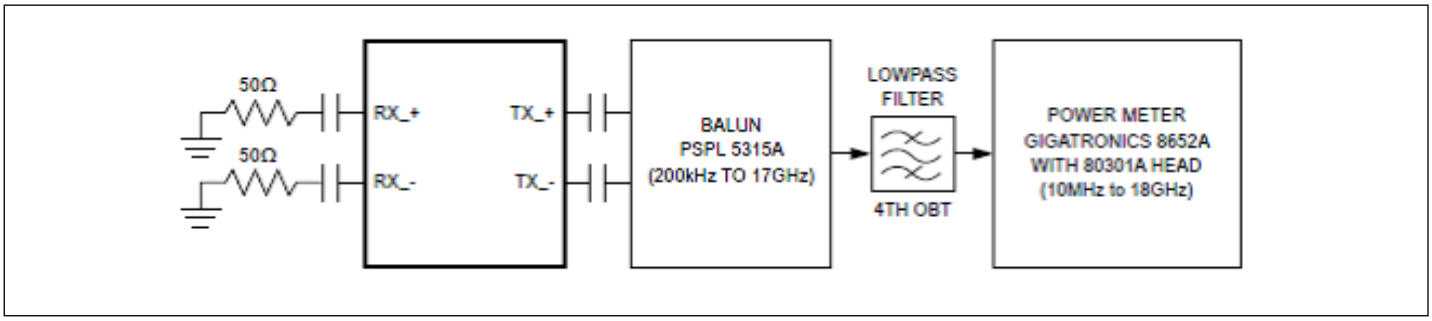



**Figure2. Noise test configuration**

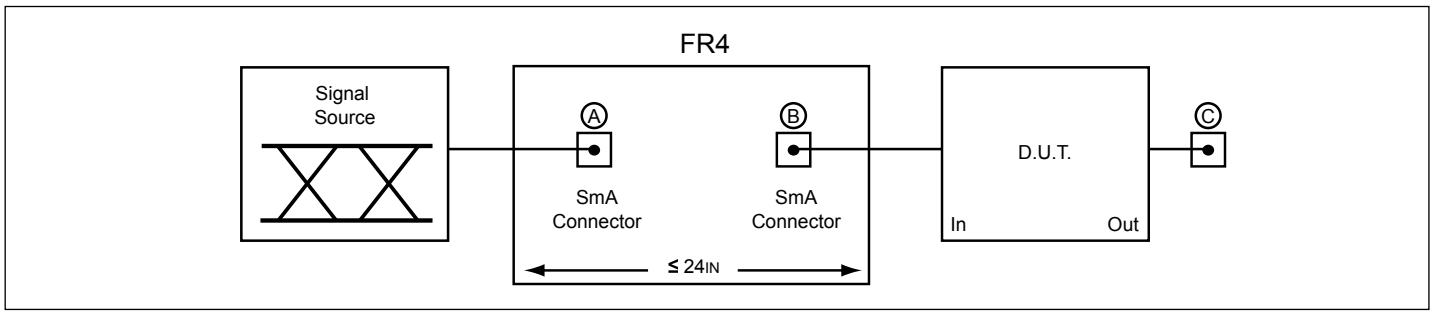
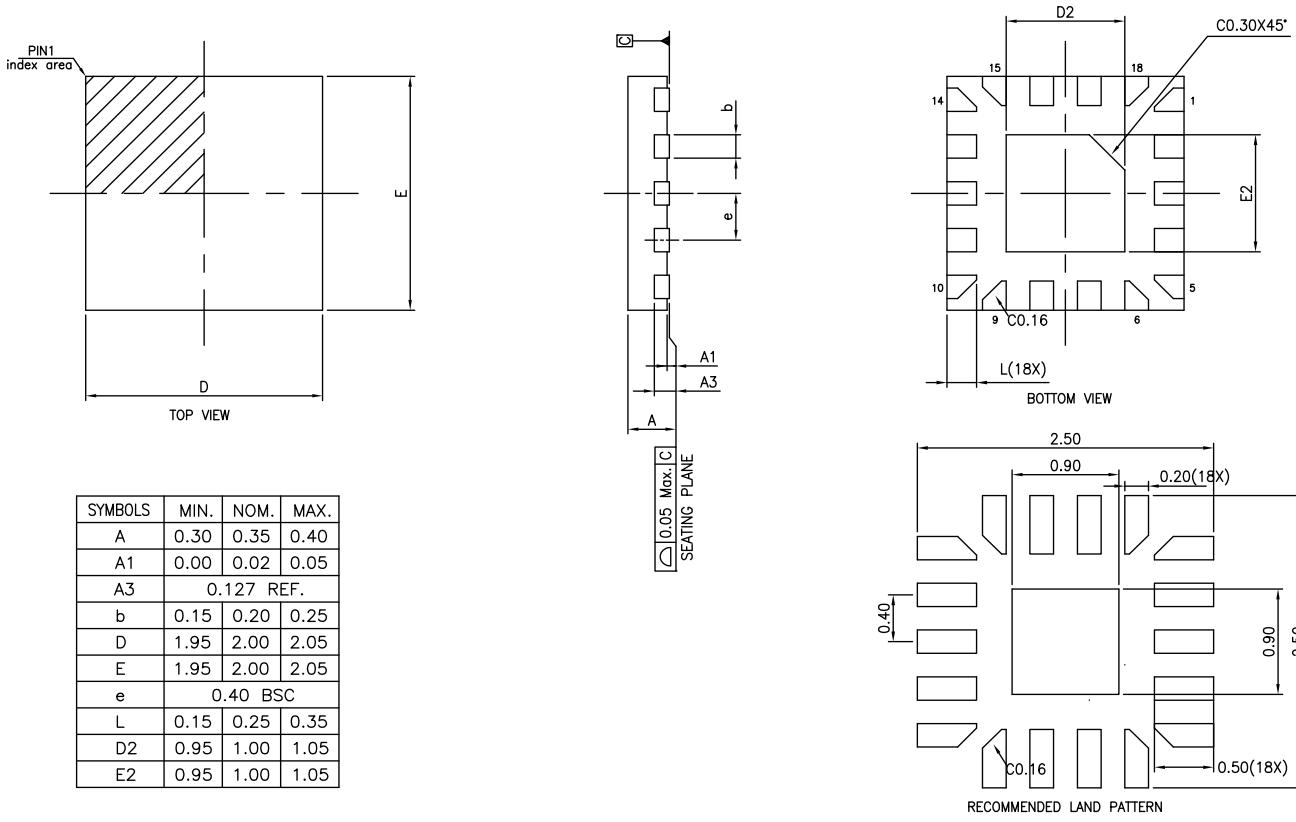



**Figure3. Test Condition Referenced in the Electrical Characteristic Table**

## Packaging Mechanical: 18-pin X2QFN




| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.30 | 0.35 | 0.40 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.127 REF. | |
| b | 0.15 | 0.20 | 0.25 |
| D | 1.95 | 2.00 | 2.05 |
| E | 1.95 | 2.00 | 2.05 |
| e | | 0.40 BSC | |
| L | 0.15 | 0.25 | 0.35 |
| D2 | 0.95 | 1.00 | 1.05 |
| E2 | 0.95 | 1.00 | 1.05 |

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. REFER JEDEC MO-288
3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY. MESH STENCIL DESIGN IS RECOMMENDED.

PERICOM Enabling Serial Connectivity

DATE: 03/31/14

DESCRIPTION: 18-Pin, X2QFN 2X2mm

PACKAGE CODE: XUA (XUA18)

DOCUMENT CONTROL #: PD-2184 REVISION: –

14-0039

**For latest package info.**

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

## Ordering Information

| Ordering Number | Package Code | Package Description |
|---|---|---|
| PI3EQX1001XUAEX | XUA | 18-Pin, 2X2mm (X2QFN) |

**Notes:**

- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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