PIC18(L)F26/45/46/55/56K42 Family Silicon Errata and Data Sheet Clarification

The PIC18(L)F26/45/46/55/56K42 family devices that you have received conform functionally to the current Device Data Sheet (DS40001919**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F26/45/46/55/56K42 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F26/45/46/55/56K42 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>(1), (2)	Revision ID for Silicon Revision	
		A1	A2
PIC18F26K42	6C60h	A001	A002
PIC18F45K42	6C20h	A001	A002
PIC18F46K42	6C00h	A001	A002
PIC18F55K42	6BC0h	A001	A002
PIC18F56K42	6BA0h	A001	A002
PIC18LF26K42	6DA0h	A001	A002
PIC18LF45K42	6D60h	A001	A002
PIC18LF46K42	6D40h	A001	A002
PIC18LF55K42	6D00h	A001	A002
PIC18LF56K42	6CE0h	A001	A002

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the *"PIC18(L)F26/45/46/55/56K42 Memory Programming Specification"* (DS40001886) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)	
				A1	A2
Electrical Specifications	SMBus 2.0	1.1	SMBus 2.0 logic levels.	X	
	SMBus 3.0	1.2	SMBus 3.0 logic levels.	X	X
	Min V_{DD} Specification for LF Devices	1.3	V_{DDMIN} for LF devices is 2.0V.	X	X
Signal Measurement Timer (SMT)	MFINTOSC Clock Sources into SMT	2.1	MFINTOSC clock sources into the SMT are not functional.	X	X
DMA	DMA Reads from Data EEPROM	3.1	DMA reads from Data EEPROM does not operate.	X	
	DMA in Doze Mode	3.2	DMA transfers may not work when CPU is in Doze mode.	X	X
UART	BRGS Select	4.1	BRGS Select feature not functional in DALI mode.		X
UART	Stop Bit Interrupt Flag	4.2	Stop Bit interrupt flag functionality not available.	X	
NVM Control	WRERR Bit Functionality	5.1	WRERR bit cannot be cleared in hardware after being set once.	X	X
WWDT	WWDT Operation in Doze Mode	6.1	Window violation occurs when WWDT operated in Doze mode.	X	X
Power-Saving Operation Modes	Low-Power Sleep Mode	7.1	Low-power Sleep mode does not operate at 3.0v<V_{DD}<3.6v.	X	X
ADC2	ADC in Precharge State	8.1	ADC shorts briefly in precharge state when the corresponding analog pin is selected as output.	X	
	Burst Average Mode Double Sampling	8.2	The ADC^2 does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Electrical Specifications

1.1 SMBus 2.0

The SMBus 2.0 VIL specification (Parameter D304) at 125°C is 0.7V.

Work around

None.

Affected Silicon Revisions

A1	A2						
X							

1.2 SMBus 3.0

The SMBus 3.0 VIL specification (Parameter D305) is temperature and VDD dependent. Refer to the table below.

Temperature	VDD	D305 SMBus 3.0 VIL Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.7V
125°C	1.8V	0.5V
125°C	5.5V	0.7V

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

1.3 Min VDD Specification for LF Devices

VDDMIN for LF devices (Parameter D002) is 2.0V.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: Signal Measurement Timer (SMT)

2.1 MFINTOSC Clock Sources into SMT

The Signal Measurement Timer does not operate when MFINTOSC is selected as the clock source (i.e. CSEL = `0b100` and `0b101`).

Work around

The MFINTOSC does not start up automatically. User software needs to manually enable the MFINTOSC by setting the MFOEN bit in the OSCCEN register. The MFINTOSC will remain enabled as long as MFOEN bit is set.

Affected Silicon Revisions

A1	A2						
X	X						

3. Module: DMA

3.1 DMA Reads from Data EEPROM

The DMA modules do not operate when CPU is in Doze mode (DOZEN = 1 in CPUDOZE register).

Work around

None. NVMCON reads work as described.

Affected Silicon Revisions

A1	A2						
X							

3.2 DMA in Doze Mode

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

4. Module: UART

4.1 Baud Rate Generator Speed Select

The Baud Rate Generator Speed Select feature (BRGS bit in the UxCON0 register) in DALI mode is not functional. The Baud Rate Generator always operates at normal speed with 16 baud clocks per bit in DALI mode.

Work around

None.

Affected Silicon Revisions

A1	A2						
	X						

4.2 Stop Bit Interrupt Flag

Stop Bit interrupt flag functionality is not available in the CERIF bit in revision A1.

Work around

Use Timer2 with HLT and connect the UART RX port to the timer Reset trigger. Set the time-out period to the desired Stop bit time (for DALI mode, this is equivalent to two Stop bits at 1200 baud = 1.66 ms). When the Stop bit is received, the timer times out notifying end of data.

Affected Silicon Revisions

A1	A2						
X							

5. Module: NVM Control

5.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

6. Module: WWDT

6.1 WWDT Operation in Doze Mode

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT even though the window is open and armed.

Work around

Do not operate the WWDT in Doze mode.

Affected Silicon Revisions

A1	A2						
X	X						

7. Module: Power-Saving Operation Modes

7.1 Low-Power Sleep Mode in F Devices

The F device resets when waking up from Sleep while in Low-Power mode (VREGPM = 1 in VREGCON register) at 3.1V < V_{DD} < 3.3V.

Work around

a) If wake-up from Sleep is needed at 3.1V < V_{DD} < 3.3V, operate the F device in Normal Power mode (VREGPM = 0).

b) If wake-up from Sleep is needed at 3.1V < V_{DD} < 3.3V, enable the Fixed Voltage Reference (EN = 1 in FVRCON register). This increases the current in Sleep mode by typically 7 µA.

Affected Silicon Revisions

A1	A2						
X	X						

8. Module: ADC^2

8.1 ADC in Precharge State

During the precharge state, if the analog pin on which the ADC conversion is performed is selected to be an output (such as LATx or ADGRDx), there is a 20 ns short between pull-up/down and the external low/high states, resulting in an inaccurate ADC conversion reading.

Work around

None

Affected Silicon Revisions

A1	A2						
X							

8.2 Burst Average Mode Double Sampling

When the ADC^2 is operated in Burst Average mode (MD = 0b011 in ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

Work around

When operating the ADC^2 in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the stop-on-interrupt bit (SOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADC^2 as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC^2 in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register) compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A1	A2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001919**B**):

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

Power-Down Current

Table 44-5 contains incorrect ADC power-down current. The correct table is as follows:

TABLE 44-5: POWER-DOWN CURRENT (I_{PD})(1,2)

PIC18LF27/47/57K42				Standard Operating Conditions (unless otherwise stated)					
PIC18F27/47/57K42				Standard Operating Conditions (unless otherwise stated) VREGPM = 1					
Param. No.	Symbol	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions	
								V_{DD}	Note
D200	I_{PD}	I_{PD} Base	—	0.07	2	10.5	µA	3.0V	
D200 D200A	I_{PD}	I_{PD} Base	—	0.4	4	12	µA	3.0V	
			—	20	38	42	µA	3.0V	VREGPM = 0
D201	I_{PD_WDT}	Low-Frequency Internal Oscillator/WDT	—	0.9	3.2	11.2	µA	3.0V	
D201	I_{PD_WDT}	Low-Frequency Internal Oscillator/WDT	—	1.1	3.2	13	µA	3.0V	
D202	I_{PD_SOSC}	Secondary Oscillator (SOSC)	—	0.75	6	14	µA	3.0V	LP mode
D202	I_{PD_SOSC}	Secondary Oscillator (SOSC)	—	1.0	7	15	µA	3.0V	LP mode
D203	I_{PD_FVR}	FVR	—	45	74	75	µA	3.0V	FVRCON = 0x81 or 0x84
D203	I_{PD_FVR}	FVR	—	40	70	76	µA	3.0V	FVRCON = 0x81 or 0x84
D204	I_{PD_BOR}	Brown-out Reset (BOR)	—	9.4	14	18	µA	3.0V	
D204	I_{PD_BOR}	Brown-out Reset (BOR)	—	9.4	15	18	µA	3.0V	
D205	I_{PD_LPBOR}	Low-Power Brown-out Reset (LPBOR)	—	0.2	3	11	µA	3.0V	
D206	I_{PD_HLVD}	High/Low Voltage Detect (HLVD)	—	9.5	14.8	18	µA	3.0V	
D206	I_{PD_HLVD}	High/Low Voltage Detect (HLVD)	—	9.7	14.2	17	µA	3.0V	
D207	**I_{PD_ADCA}**	**ADC – Non-Converting**	**—**	**0.1**	**2**	**10.5**	**µA**	**3.0V**	**ADC not converting (4)**
D207	**I_{PD_ADCA}**	**ADC – Non-Converting**	**—**	**0.1**	**4**	**12**	**µA**	**3.0V**	**ADC not converting (4)**
D208	I_{PD_CMP}	Comparator	—	33	49	50	µA	3.0V	
D208	I_{PD_CMP}	Comparator	—	30	49	50	µA	3.0V	

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{DD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max. values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to V_{SS}.

3: All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.

4: ADC clock source is FRC.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (06/2017)

Initial release of this document.

Rev B Document (10/2017)

Added Module 3: DMA to Silicon Errata Issues. Other minor corrections.

Rev C Document (06/2018)

Updated Table 1 and Table 2; Added Module 4: UART; Module 3.2; Module 5: NVM Control; Module 6: WWDT; Module 7: Power-Saving Operation Modes; Added Module 8: ADC

Data Sheet Clarifications: Added Module 1: Electrical Specifications.

Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

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